SSD2119

Advance Information

320 RGB x 240 TFT LCD Driver
Integrated Power Circuit, Source and Gate Driver and RAM

IC Revision history of SSD2119 Specification

Version	Change Items	Effective Date
0.10	1st Release P.76 Application Circuit updated P.80 Figure 19-4 – ITO and FPC connection example added P.26 Remove SPI Interface from CS P.26 Add SCS for SPI Chip Select, CS/SCS – chip select pin for both parallel and serial interface. P.66 All Waveform pin name is updated P.13 PadCo pin name of pad# 266 & 269 is updated P.66 Figure 13.1, 13.2 13.3 are updated.	31-Jan-08
0.20	P.10 Alignment Mark Updated base on padco v4.0 –	26-Feb-08
0.30	P.265 Padco updated to v5.0 on Table 5-2 P.63 Test condition (Booster Ratio) added for I_{dp}(8 color) on page 13 P.72 Table 15-1 is updated to 1000 18-bit 6800 1001 9-bit 6800 1010 18-bit 8080 1011 9-bit 8080 P.1-80 "CONFIDENTIAL" water mark being removed. P.267 Pin name updated for pin 308 to 327 P.62 Operating Temperature update to -40 to +85 ^{o}C for Section 11(page 13) and Section 12(page 13).	06-Mar-08
0.40	P.10 Die Size(No Scribe) updated to 23724 x 780 um^2 P.10 Die Thickness updated to 400 ± 25 um P.80 Figure 19-4 Pin 229 to Pin 242 Updated	18-Mar-08
0.41	P.32 R01h, R44h, R45h, R46h, R48h, R49h, R4Ah, R4Bh, R4Eh, R4Fh Command Updated	17-Apr-08
0.42	P.27 D9-D16 is used for RGB, D12 short to D17 for 65K color P64-66 Updated AC Timing Diagrams P.49 Updated OTP programming sequence P.52 Updated RAM address set (R4Eh-R4Fh) Swapped X and Y position	23-Jul-08
0.43	P. 28-29 Updated SPI interface P.74 Updated SPI bit mapping P.52 Updated OTP P.68 Updated Tas and Tah definition P.32 Updated R11h POR to 6230h P.41 Updated R03h POR to 6ª64h P.45 Updated Frame Frequency formula P.50 Updated diagram address to 13F, EFH. P.56 Updated Conditions to HEA[8:0]<= 13FH, VEA[7:0]<=EFH . P.56-58 Updated all VEA to [7:0] and all HEA to [8:0]	08-Aug-08
0.44	P.67-68 Updated (Tcycle = Min. 100ns, PWcsl = PWcsh = Min. 50ns) to Tcycle = Min. 75ns, PWcsl = Min.40ns PWcsh = Min. 25ns added Note: CS can be pulled low during the write cycle, only /RW is needed to be toggled P.70-71 Added RGB Timing P.36 Change GS to TB P.12 Change OE to DEN in table 5-2 P.12 Remove G0 in table 5-2 P.65-70 Corrected VDDIO from 1.65V to 1.4V P.76 Added Mapping for Writing Pixel Data in SPI mode	19-Aug-08
0.45	P.70 Updated RGB Timing Characteristics P.62 Updated Gama Ladder Resistor table format P.12-22, 36, 59-60, 80, 84 Fixed format of Table 5-2, TB Table, Grayscale Amplifier, Power supply block diagram and Figure 19-4	20-Aug-08

Version	Change Items	Effective Date
	P. 68-70 Updated all temperature to -40 to 85°C	
0.46	P.74 Updated Table 15.2 The Function of 6800-series parallel interface P.52 Updated Internal Oscillator Frequency P.76 Updated Table 15.4 Mapping for Writing Pixel Data in generic mode P.79-80 Updated 16.2 Display OFF Sequence and 16.3 Sleep Mode Display Sequence P.35 Updated Device Code P.33 Remove SR(status read) register P.87 Added Section 21 OTP explanation P.53 Added OTP sequence step 4 "Turn on the display as normal to 65k/262k color mode" P.34, 56 Updated GDDRAM X Y address	24-Sep-08
0.47	P52. Add Deep sleep mode command R12 and correct R10 description P37. Add R12.	06-Oct-08
0.48	P.50 Corrected Dmode=1 : Display engine will be clocked by DOTCLK pin and onchip oscillator will be off (POR, if PS:00xx) Dmode=0 : Display engine will be clocked by on chip oscillator and ignore DOTCLK pin P.71 Corrected Table 13-2: RGB Timing Characteristics Dotclock period to ns P.48 Swapped R12 and R10 in deep sleep sequence	13-Nov-08
0.49	P.80, 82 Added Halt, Deep sleep sequence. P.67 Updated power consumption information of sleep mode P.67 Added power consumption information of Halt and Deep sleep mode P.67 Added "The leakage current is below 100uA if Reset keeps at low state when power on" P.67 Updated deep sleep mode max current to 15uA P.26 RESB pin description amend to "An external reset pulse to RESB is required for power up (sequence)." This change is to prevent unexpected internal RESET by excessive electrical stress.	26-Nov-08
0.50	P.52 Corrected R1EH VCM default to x2B P.53 Added analogue setting register description P.48-49 Added VSH[2:0] and HVCI of R12h P.68-69 Change read cycle to 450ns P.70 Updated Ihalt max to 120uA P.78 Added reset pulse timing P.52 Updated "GDDRAM data and instruction setting needed to be sent again after exit deep sleep mode" to "DDRAM data needed to be sent again after exit deep sleep mode" P.94 Added Chip tray information	16-Dec-08
1.0	Advanced information P.33, 48 Remove HVCI bit in R12h P.48, 87 Corrected R12h code to 2999h P.33, 51 Corrected R15h POR to B010h P.35 Correct read ID code from 1919h to 9919h P.12, 91 Swapped CYN and CYP pins P.33, 52, 53Add R16 and R17 register P.57 Add Program voltage range – 14.5 to 15.5 P.57 Added "It is possible to skip step3 and step4" and changed "Step 4-9" to "Step 5-9" P.34, 54 Added R20h Uniformity settings	23-Jan-09
1.1	P.11 Updated ordering part number as SSD2119Z7 P.73 Removed (/CS) from tr and tf P.73 Added VCI and Reset pin to diagram P.74 Removed (/CS) from tr and tf P.75 Added VCI and Reset pin to diagram P.78 Updated Fig13-5 as power up sequence for RGB mode P.87 Added timing to display off sequence	13-Feb-09

Version	Change Items	Effective Date
	P.96 Added Chiptray diagram of SSD2119Z7 P.95 Corrected shifted VCHS to Gnd wire to proper position P.47 Added notes below table of R0CH	
1.2	P.52 Added “Note: ID and AM functions are not supported in RGB mode” P.50 Added “DenMode=1 (DEN signal is necessary); DenMode=0 (DEN pin must connect to VDDIO)”	20-Mar-09
1.3	P.8 Changed from "Charge sharing function for step-up circuits" to "charge sharing function P.26 Corrected 3n to 3n+3 P.34 Removed "Note: The POR value of REV, BGR, RL are determined by the corresponding hardware pin state. The software bit setting will override hardware setting if this command is sent." P.62 Corrected to 240 row in R41h/R42h P.62 Corrected Ensure that SS1[8:0] ≤ SE1[8:0] ≤ EFH. (R48h/R49h) P.63 Corrected "Ensure that SS1[8:0] ≤ SE1[8:0] ; SS2[8:0] ≤ SE2[8:0] ≤ EFH. (R4Ah/R4Bh) P.65 Corrected "Partial Display Mode" to EFh P.82 Corrected the no. of gate/source in section "GDDRAM Address".	08-May-09
1.4	P.13 Die size (no scribe; seal ring only) corrected from 23850 x 730 μm2 to 23724 x 780 μm2 P.69 Add remark in DC table12: The setting of VLCD63 is needed to below 0.5V of VCIX2. It is the prevention of VCIX2 noise to couple to VLCD63 gamma voltage	09-Jun-09

CONTENTS

TABLES

FIGURES

1 GENERAL DESCRIPTION

SSD2119 is an all in one TFT LCD Driver that integrated the power circuits, gate driver and source driver into a single chip. It can drive up to 262k color amorphous TFT panel with resolution of 320 RGB x 240.

It also integrated the controller function and consists of up to 172,800 bytes (320 x 240 x 18 / 8) Graphic Display Data RAM (GDDRAM) such that it interfaced with common MCU through 8/9/16/18-bits 6800-series / 8080-series compatible Parallel Interface or Serial Interface and stored the data in the GDDRAM. Auxiliary 18-/6- bit video interface (VSYNC, HSYNC, DOTCLK, DEN) are integrated into SSD2119 for animation image display.

SSD2119 embeds DC-DC Converter and Voltage generator to provide all necessary voltage required by the driver with minimum external components. A Common Voltage Generation Circuit is included to drive the TFT-display counter electrode. An Integrated Gamma Control Circuit is also included that can be adjusted by software commands to provide maximum flexibility and optimal display quality.

SSD2119 can be operated down to 1.4V and provide different power save modes. It is suitable for any portable battery-driven applications requiring long operation period and compact size.

2 FEATURES

- 320RGBx240 single chip controller driver IC for 262k color amorphous TFT LCD
- Power Supply
  - VDDIO = 1.4V – 3.6V (I/O Interface)
  - VCI = 2.5V – 3.6V (power supply for internal analog circuit)
- Output Voltages
  - Gate Driver:
    - VGH-GND = 9V ~ 18V
    - VGL-GND = -6 ~ -15V
    - VGH-VGL = 30Vp-p max.
  - Source Driver:
    - V0 – V63 = 0 – 6V max.
  - VCOM drive:
    - VCOMH = 3.0V ~ 5.0V
    - VCOML = -1.0V ~ -3.0V
    - VCOMA = 6V max.
- System Interface
  - 8/ 9/ 16/ 18-bit 6800-series / 8080-series Parallel Interface
  - Serial Peripheral Interface (SPI)
- Moving picture display interface
  - 18-/6-bit RGB interface (DEN, DOTCLK, HSYNC, VSYNC, DB[17:0])
  - VSYNC interface (system interface + VSYNC)
  - WSYNC interface (system interface + WSYNC)
- Support low power consumption:
  - Low voltage supply
  - Low current sleep mode
  - 8-color display mode for power saving
  - Charge sharing functions
- High-speed RAM addressing functions
  - RAM write synchronization function
  - Window address function
  - Vertical scrolling function
  - Partial display function
- Internal power supply circuit
  - Voltage generator
  - DC-DC converter up to 6x/-5x
- Built-in internal oscillator
- Internal GDDRAM capacity: 172800 Byte
- Support Frame and Line inversion AC drive
- TFT storage capacitance: Cs on common
- Support source and gate scan direction control
- Programmable gamma correction curve
- 4 Preset gamma correction curve
- Built-in Non Volatile Memory for VCOM calibration
- Support flexible arrangement of gate circuits on both sides of the glass substrate

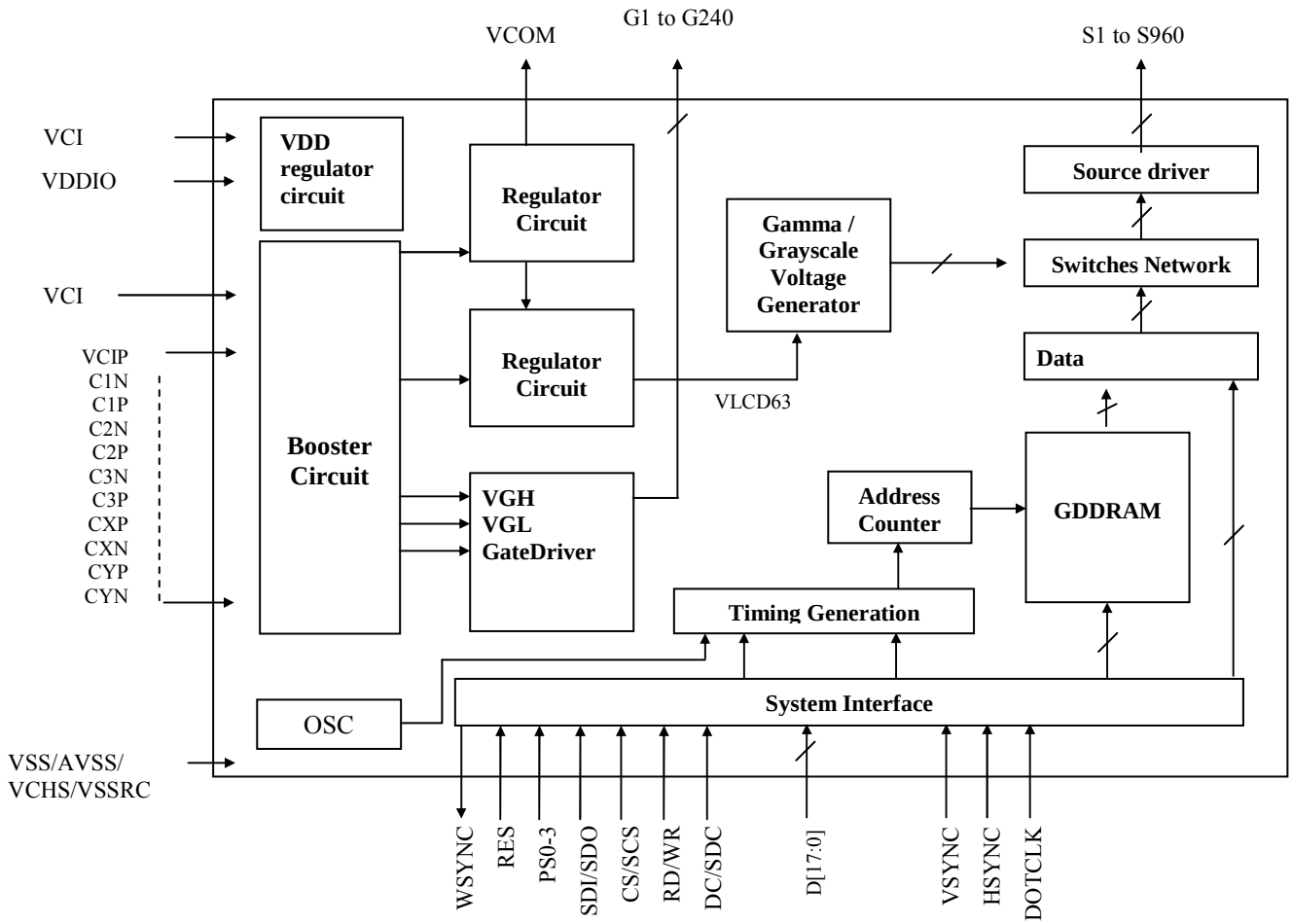
3 ORDERING INFORMATION

Table 3-1: Ordering Information

Ordering Part Number	Source output channel	Gate output channel	Package Form	Reference	Remark
SSD2119Z7	320 x 3 (960)	240	Gold Bump Die		

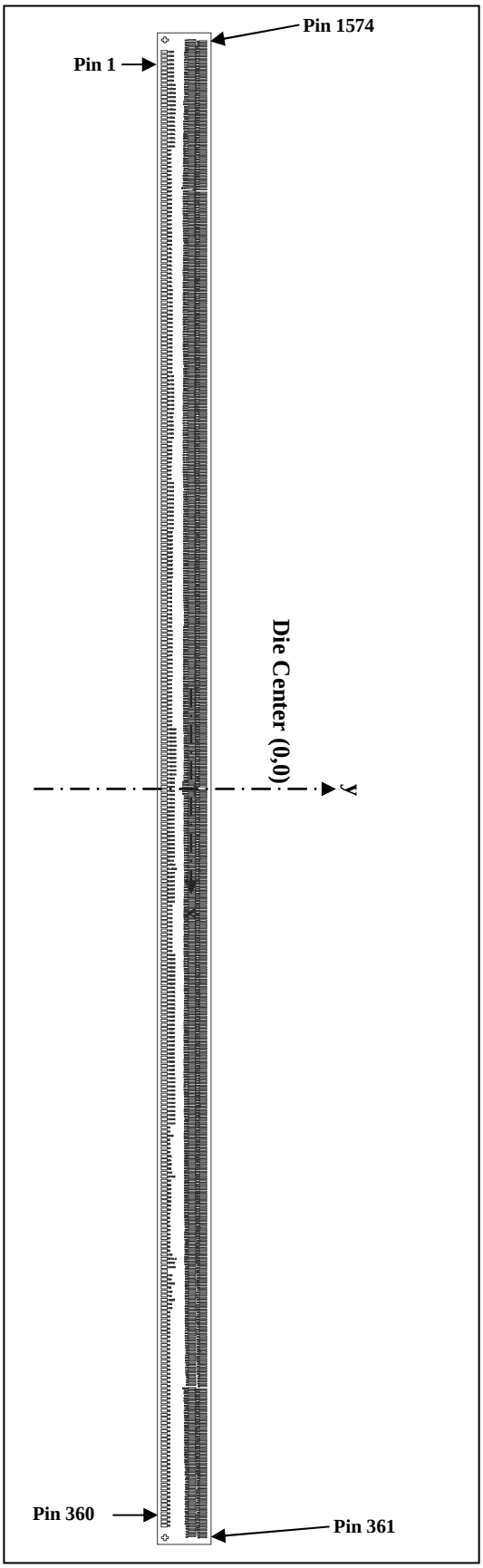
4 BLOCK DIAGRAM

Figure 4-1: SSD2119 Block Diagram



5 DIE PAD FLOOR PLAN

Figure 5-1: SSD2119 Die Pad Floor Plan



Note
(1) Diagram showing the die face up.
(2) Coordinates are referenced to center of the chip.
(3) Coordinate units and size of all alignment marks are in um.
(4) All alignment keys do not contain gold bump.

Figure 5-2: Alignment Marks

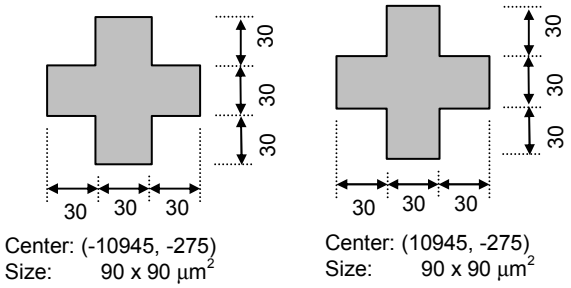


Figure 5-3: Output Pad Pitch (Pad 361 - 1574)

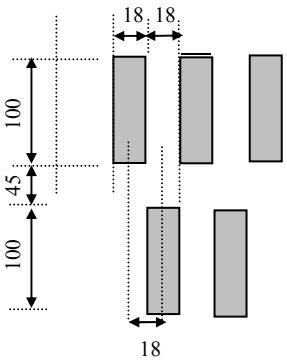


Table 5-1: Die Information

Die Size (no scribe)	23724 x 780 um^2
Die Thickness	400 ± 25 um
Typical Bump Height	15 um
Bump Co-planarity (within die)	≤ 2 um
Bump Size 1	40 x 80 μm^2 (Pin 1 – 360)
Pad Pitch 1	60 μm
Bump Size 2	18 x 100 μm^2 (Pin 361 – 1574)
Pad Pitch 2	18 μm stagger

Table 5-2: SSD2119 Bump Die Pad Coordinates (Bump Centre)

Note: IC material temperature expansion factor is 2.6ppm, customer should take into account during panel design

Pad #	Pad Name	X-pos	Y-pos	Pad #	Pad Name	X-pos	Y-pos	Pad #	Pad Name	X-pos	Y-pos
1	VCOM	-10770	-286	51	VGL	-7770	-286	101	CXP	-4770	-286
2	VCOM	-10710	-286	52	VGL	-7710	-286	102	CXP	-4710	-286
3	VCOM	-10650	-286	53	VGL	-7650	-286	103	CXP	-4650	-286
4	VCOM	-10590	-286	54	VGL	-7590	-286	104	CXP	-4590	-286
5	VCOM	-10530	-286	55	VGL	-7530	-286	105	CXP	-4530	-286
6	VCOM	-10470	-286	56	VGL	-7470	-286	106	VCHS	-4470	-286
7	VCOM	-10410	-286	57	VGL	-7410	-286	107	VCHS	-4410	-286
8	VCOM	-10350	-286	58	VGL	-7350	-286	108	VCHS	-4350	-286
9	VCOMH	-10290	-286	59	VGH	-7290	-286	109	VCHS	-4290	-286
10	VCOMH	-10230	-286	60	VGH	-7230	-286	110	VCHS	-4230	-286
11	VCOMH	-10170	-286	61	VGH	-7170	-286	111	VCHS	-4170	-286
12	VCOMH	-10110	-286	62	VGH	-7110	-286	112	VCHS	-4110	-286
13	VCOMH	-10050	-286	63	VGH	-7050	-286	113	VCHS	-4050	-286
14	VCOMH	-9990	-286	64	VGH	-6990	-286	114	VCHS	-3990	-286
15	VCOMH	-9930	-286	65	VGH	-6930	-286	115	VCHS	-3930	-286
16	VCOMH	-9870	-286	66	VGH	-6870	-286	116	VCHS	-3870	-286
17	VCOML	-9810	-286	67	VGH	-6810	-286	117	VCHS	-3810	-286
18	VCOML	-9750	-286	68	VGH	-6750	-286	118	VCIP	-3750	-286
19	VCOML	-9690	-286	69	VGH	-6690	-286	119	VCIP	-3690	-286
20	VCOML	-9630	-286	70	VGH	-6630	-286	120	VCIP	-3630	-286
21	VCOML	-9570	-286	71	VSS	-6570	-286	121	VCIP	-3570	-286
22	VCOML	-9510	-286	72	VSS	-6510	-286	122	VCIP	-3510	-286
23	VCOML	-9450	-286	73	VSS	-6450	-286	123	VCIP	-3450	-286
24	VCOML	-9390	-286	74	VSS	-6390	-286	124	VCIP	-3390	-286
25	C1P	-9330	-286	75	VSS	-6330	-286	125	VCIP	-3330	-286
26	C1P	-9270	-286	76	VSS	-6270	-286	126	VCIP	-3270	-286
27	C1P	-9210	-286	77	VSS	-6210	-286	127	VCIP	-3210	-286
28	C1P	-9150	-286	78	VSS	-6150	-286	128	VCIP	-3150	-286
29	C1N	-9090	-286	79	VSS	-6090	-286	129	VCIP	-3090	-286
30	C1N	-9030	-286	80	AVSS	-6030	-286	130	VCI	-3030	-286
31	C1N	-8970	-286	81	AVSS	-5970	-286	131	VCI	-2970	-286
32	C1N	-8910	-286	82	AVSS	-5910	-286	132	VCI	-2910	-286
33	C2P	-8850	-286	83	AVSS	-5850	-286	133	VCI	-2850	-286
34	C2P	-8790	-286	84	AVSS	-5790	-286	134	VCI	-2790	-286
35	C2P	-8730	-286	85	AVSS	-5730	-286	135	VCI	-2730	-286
36	C2P	-8670	-286	86	AVSS	-5670	-286	136	VCI	-2670	-286
37	C2N	-8610	-286	87	AVSS	-5610	-286	137	VCI	-2610	-286
38	C2N	-8550	-286	88	AVSS	-5550	-286	138	VCI	-2550	-286
39	C2N	-8490	-286	89	VCIM	-5490	-286	139	VCI	-2490	-286
40	C2N	-8430	-286	90	VCIM	-5430	-286	140	VCI	-2430	-286
41	C3P	-8370	-286	91	VCIM	-5370	-286	141	VCI	-2370	-286
42	C3P	-8310	-286	92	VCIM	-5310	-286	142	CYN	-2310	-286
43	C3P	-8250	-286	93	VCIM	-5250	-286	143	CYN	-2250	-286
44	C3P	-8190	-286	94	VCIM	-5190	-286	144	CYN	-2190	-286
45	C3N	-8130	-286	95	VCIM	-5130	-286	145	CYN	-2130	-286
46	C3N	-8070	-286	96	CXN	-5070	-286	146	CYN	-2070	-286
47	C3N	-8010	-286	97	CXN	-5010	-286	147	CYN	-2010	-286
48	C3N	-7950	-286	98	CXN	-4950	-286	148	CYN	-1950	-286
49	VGL	-7890	-286	99	CXN	-4890	-286	149	CYN	-1890	-286
50	VGL	-7830	-286	100	CXN	-4830	-286	150	CYN	-1830	-286

Pad #	Pad Name	X-pos	Y-pos	Pad #	Pad Name	X-pos	Y-pos	Pad #	Pad Name	X-pos	Y-pos
151	CYN	-1770	-286	201	DUMMY	1230	-286	251	VSSRC	4230	-286
152	CYN	-1710	-286	202	DUMMY	1290	-286	252	VSSRC	4290	-286
153	CYN	-1650	-286	203	DUMMY	1350	-286	253	VSSRC	4350	-286
154	CYP	-1590	-286	204	DUMMY	1410	-286	254	VSSRC	4410	-286
155	CYP	-1530	-286	205	DUMMY	1470	-286	255	VSSRC	4470	-286
156	CYP	-1470	-286	206	DUMMY	1530	-286	256	VSSRC	4530	-286
157	CYP	-1410	-286	207	DUMMY	1590	-286	257	VSSRC	4590	-286
158	CYP	-1350	-286	208	DUMMY	1650	-286	258	VSSRC	4650	-286
159	CYP	-1290	-286	209	VSS	1710	-286	259	VSSRC	4710	-286
160	CYP	-1230	-286	210	VSS	1770	-286	260	VSSRC	4770	-286
161	CYP	-1170	-286	211	VSS	1830	-286	261	VSSRC	4830	-286
162	CYP	-1110	-286	212	VSS	1890	-286	262	VSSRC	4890	-286
163	CYP	-1050	-286	213	VSS	1950	-286	263	NC	4950	-286
164	CYP	-990	-286	214	VSS	2010	-286	264	NC	5010	-286
165	CYP	-930	-286	215	VSS	2070	-286	265	RESB	5070	-286
166	VCIX2G	-870	-286	216	VSS	2130	-286	266	DC/SDC	5130	-286
167	VCIX2G	-810	-286	217	VSS	2190	-286	267	RD	5190	-286
168	VCIX2G	-750	-286	218	VSS	2250	-286	268	RW	5250	-286
169	VCIX2G	-690	-286	219	VSS	2310	-286	269	CS/SCS	5310	-286
170	VCIX2G	-630	-286	220	VSS	2370	-286	270	SCL	5370	-286
171	VCIX2G	-570	-286	221	VREGC	2430	-286	271	SCL	5430	-286
172	VCIX2G	-510	-286	222	VREGC	2490	-286	272	SDO	5490	-286
173	VCIX2G	-450	-286	223	VREGC	2550	-286	273	SDI	5550	-286
174	VCIX2G	-390	-286	224	VREGC	2610	-286	274	VSS	5610	-286
175	VCIX2G	-330	-286	225	VREGC	2670	-286	275	WSYNC	5670	-286
176	VCIX2G	-270	-286	226	VREGC	2730	-286	276	D17	5730	-286
177	VCIX2G	-210	-286	227	VREGC	2790	-286	277	D16	5790	-286
178	VCIX2	-150	-286	228	VREGC	2850	-286	278	D15	5850	-286
179	VCIX2	-90	-286	229	VCORE	2910	-286	279	D14	5910	-286
180	VCIX2	-30	-286	230	VCORE	2970	-286	280	D13	5970	-286
181	VCIX2	30	-286	231	VCORE	3030	-286	281	D12	6030	-286
182	VCIX2	90	-286	232	VCORE	3090	-286	282	D11	6090	-286
183	VCIX2	150	-286	233	VCORE	3150	-286	283	D10	6150	-286
184	VCIX2	210	-286	234	VCORE	3210	-286	284	D9	6210	-286
185	VCIX2	270	-286	235	VDDIO	3270	-286	285	D8	6270	-286
186	CDUM0	330	-286	236	VDDIO	3330	-286	286	D7	6330	-286
187	CDUM0	390	-286	237	VDDIO	3390	-286	287	D6	6390	-286
188	CDUM0	450	-286	238	VDDIO	3450	-286	288	D5	6450	-286
189	CDUM0	510	-286	239	VDDIO	3510	-286	289	D4	6510	-286
190	CDUM0	570	-286	240	VDDIO	3570	-286	290	D3	6570	-286
191	CDUM0	630	-286	241	VDDIO	3630	-286	291	D2	6630	-286
192	CDUM0	690	-286	242	VDDIO	3690	-286	292	D1	6690	-286
193	CDUM0	750	-286	243	VDDIO	3750	-286	293	D0	6750	-286
194	CDUM0	810	-286	244	VDDIO	3810	-286	294	VSS	6810	-286
195	CDUM0	870	-286	245	VDDIO	3870	-286	295	DOTCLK	6870	-286
196	CDUM0	930	-286	246	VDDIO	3930	-286	296	HSYNC	6930	-286
197	CDUM0	990	-286	247	VDDIO	3990	-286	297	VSYNC	6990	-286
198	EXVR	1050	-286	248	VDDIO	4050	-286	298	DEN	7050	-286
199	VCOMR	1110	-286	249	VDDIO	4110	-286	299	VSS	7110	-286
200	VLCD63	1170	-286	250	VDDIO	4170	-286	300	PS0	7170	-286

Pad #	Pad Name	X-pos	Y-pos	Pad #	Pad Name	X-pos	Y-pos	Pad #	Pad Name	X-pos	Y-pos
301	VDDIO	7230	-286	351	NC	10230	-286	401	G81	10221	226
302	PS1	7290	-286	352	NC	10290	-286	402	G83	10203	81
303	VSS	7350	-286	353	NC	10350	-286	403	G85	10185	226
304	PS2	7410	-286	354	NC	10410	-286	404	G87	10167	81
305	VDDIO	7470	-286	355	NC	10470	-286	405	G89	10149	226
306	PS3	7530	-286	356	NC	10530	-286	406	G91	10131	81
307	VSS	7590	-286	357	NC	10590	-286	407	G93	10113	226
308	NC	7650	-286	358	NC	10650	-286	408	G95	10095	81
309	NC	7710	-286	359	NC	10710	-286	409	G97	10077	226
310	NC	7770	-286	360	NC	10770	-286	410	G99	10059	81
311	NC	7830	-286	361	G1	10941	226	411	G101	10041	226
312	NC	7890	-286	362	G3	10923	81	412	G103	10023	81
313	NC	7950	-286	363	G5	10905	226	413	G105	10005	226
314	NC	8010	-286	364	G7	10887	81	414	G107	9987	81
315	NC	8070	-286	365	G9	10869	226	415	G109	9969	226
316	NC	8130	-286	366	G11	10851	81	416	G111	9951	81
317	NC	8190	-286	367	G13	10833	226	417	G113	9933	226
318	NC	8250	-286	368	G15	10815	81	418	G115	9915	81
319	NC	8310	-286	369	G17	10797	226	419	G117	9897	226
320	NC	8370	-286	370	G19	10779	81	420	G119	9879	81
321	NC	8430	-286	371	G21	10761	226	421	G121	9861	226
322	NC	8490	-286	372	G23	10743	81	422	G123	9843	81
323	NC	8550	-286	373	G25	10725	226	423	G125	9825	226
324	NC	8610	-286	374	G27	10707	81	424	G127	9807	81
325	NC	8670	-286	375	G29	10689	226	425	G129	9789	226
326	NC	8730	-286	376	G31	10671	81	426	G131	9771	81
327	NC	8790	-286	377	G33	10653	226	427	G133	9753	226
328	NC	8850	-286	378	G35	10635	81	428	G135	9735	81
329	NC	8910	-286	379	G37	10617	226	429	G137	9717	226
330	NC	8970	-286	380	G39	10599	81	430	G139	9699	81
331	NC	9030	-286	381	G41	10581	226	431	G141	9681	226
332	NC	9090	-286	382	G43	10563	81	432	G143	9663	81
333	NC	9150	-286	383	G45	10545	226	433	G145	9645	226
334	NC	9210	-286	384	G47	10527	81	434	G147	9627	81
335	NC	9270	-286	385	G49	10509	226	435	G149	9609	226
336	NC	9330	-286	386	G51	10491	81	436	G151	9591	81
337	NC	9390	-286	387	G53	10473	226	437	G153	9573	226
338	NC	9450	-286	388	G55	10455	81	438	G155	9555	81
339	NC	9510	-286	389	G57	10437	226	439	G157	9537	226
340	NC	9570	-286	390	G59	10419	81	440	G159	9519	81
341	NC	9630	-286	391	G61	10401	226	441	G161	9501	226
342	NC	9690	-286	392	G63	10383	81	442	G163	9483	81
343	NC	9750	-286	393	G65	10365	226	443	G165	9465	226
344	NC	9810	-286	394	G67	10347	81	444	G167	9447	81
345	NC	9870	-286	395	G69	10329	226	445	G169	9429	226
346	NC	9930	-286	396	G71	10311	81	446	G171	9411	81
347	NC	9990	-286	397	G73	10293	226	447	G173	9393	226
348	NC	10050	-286	398	G75	10275	81	448	G175	9375	81
349	NC	10110	-286	399	G77	10257	226	449	G177	9357	226
350	NC	10170	-286	400	G79	10239	81	450	G179	9339	81

Pad #	Pad Name	X-pos	Y-pos	Pad #	Pad Name	X-pos	Y-pos	Pad #	Pad Name	X-pos	Y-pos
451	G181	9321	226	501	S19	8407	226	551	S69	7507	226
452	G183	9303	81	502	S20	8389	81	552	S70	7489	81
453	G185	9285	226	503	S21	8371	226	553	S71	7471	226
454	G187	9267	81	504	S22	8353	81	554	S72	7453	81
455	G189	9249	226	505	S23	8335	226	555	S73	7435	226
456	G191	9231	81	506	S24	8317	81	556	S74	7417	81
457	G193	9213	226	507	S25	8299	226	557	S75	7399	226
458	G195	9195	81	508	S26	8281	81	558	S76	7381	81
459	G197	9177	226	509	S27	8263	226	559	S77	7363	226
460	G199	9159	81	510	S28	8245	81	560	S78	7345	81
461	G201	9141	226	511	S29	8227	226	561	S79	7327	226
462	G203	9123	81	512	S30	8209	81	562	S80	7309	81
463	G205	9105	226	513	S31	8191	226	563	S81	7291	226
464	G207	9087	81	514	S32	8173	81	564	S82	7273	81
465	G209	9069	226	515	S33	8155	226	565	S83	7255	226
466	G211	9051	81	516	S34	8137	81	566	S84	7237	81
467	G213	9033	226	517	S35	8119	226	567	S85	7219	226
468	G215	9015	81	518	S36	8101	81	568	S86	7201	81
469	G217	8997	226	519	S37	8083	226	569	S87	7183	226
470	G219	8979	81	520	S38	8065	81	570	S88	7165	81
471	G221	8961	226	521	S39	8047	226	571	S89	7147	226
472	G223	8943	81	522	S40	8029	81	572	S90	7129	81
473	G225	8925	226	523	S41	8011	226	573	S91	7111	226
474	G227	8907	81	524	S42	7993	81	574	S92	7093	81
475	G229	8889	226	525	S43	7975	226	575	S93	7075	226
476	G231	8871	81	526	S44	7957	81	576	S94	7057	81
477	G233	8853	226	527	S45	7939	226	577	S95	7039	226
478	G235	8835	81	528	S46	7921	81	578	S96	7021	81
479	G237	8817	226	529	S47	7903	226	579	S97	7003	226
480	G239	8799	81	530	S48	7885	81	580	S98	6985	81
481	DUMMY	8781	226	531	S49	7867	226	581	S99	6967	226
482	DUMMY	8763	81	532	S50	7849	81	582	S100	6949	81
483	S1	8731	226	533	S51	7831	226	583	S101	6931	226
484	S2	8713	81	534	S52	7813	81	584	S102	6913	81
485	S3	8695	226	535	S53	7795	226	585	S103	6895	226
486	S4	8677	81	536	S54	7777	81	586	S104	6877	81
487	S5	8659	226	537	S55	7759	226	587	S105	6859	226
488	S6	8641	81	538	S56	7741	81	588	S106	6841	81
489	S7	8623	226	539	S57	7723	226	589	S107	6823	226
490	S8	8605	81	540	S58	7705	81	590	S108	6805	81
491	S9	8587	226	541	S59	7687	226	591	S109	6787	226
492	S10	8569	81	542	S60	7669	81	592	S110	6769	81
493	S11	8551	226	543	S61	7651	226	593	S111	6751	226
494	S12	8533	81	544	S62	7633	81	594	S112	6733	81
495	S13	8515	226	545	S63	7615	226	595	S113	6715	226
496	S14	8497	81	546	S64	7597	81	596	S114	6697	81
497	S15	8479	226	547	S65	7579	226	597	S115	6679	226
498	S16	8461	81	548	S66	7561	81	598	S116	6661	81
499	S17	8443	226	549	S67	7543	226	599	S117	6643	226
500	S18	8425	81	550	S68	7525	81	600	S118	6625	81

Pad #	Pad Name	X-pos	Y-pos	Pad #	Pad Name	X-pos	Y-pos	Pad #	Pad Name	X-pos	Y-pos
601	S119	6607	226	651	S169	5707	226	701	S219	4807	226
602	S120	6589	81	652	S170	5689	81	702	S220	4789	81
603	S121	6571	226	653	S171	5671	226	703	S221	4771	226
604	S122	6553	81	654	S172	5653	81	704	S222	4753	81
605	S123	6535	226	655	S173	5635	226	705	S223	4735	226
606	S124	6517	81	656	S174	5617	81	706	S224	4717	81
607	S125	6499	226	657	S175	5599	226	707	S225	4699	226
608	S126	6481	81	658	S176	5581	81	708	S226	4681	81
609	S127	6463	226	659	S177	5563	226	709	S227	4663	226
610	S128	6445	81	660	S178	5545	81	710	S228	4645	81
611	S129	6427	226	661	S179	5527	226	711	S229	4627	226
612	S130	6409	81	662	S180	5509	81	712	S230	4609	81
613	S131	6391	226	663	S181	5491	226	713	S231	4591	226
614	S132	6373	81	664	S182	5473	81	714	S232	4573	81
615	S133	6355	226	665	S183	5455	226	715	S233	4555	226
616	S134	6337	81	666	S184	5437	81	716	S234	4537	81
617	S135	6319	226	667	S185	5419	226	717	S235	4519	226
618	S136	6301	81	668	S186	5401	81	718	S236	4501	81
619	S137	6283	226	669	S187	5383	226	719	S237	4483	226
620	S138	6265	81	670	S188	5365	81	720	S238	4465	81
621	S139	6247	226	671	S189	5347	226	721	S239	4447	226
622	S140	6229	81	672	S190	5329	81	722	S240	4429	81
623	S141	6211	226	673	S191	5311	226	723	S241	4411	226
624	S142	6193	81	674	S192	5293	81	724	S242	4393	81
625	S143	6175	226	675	S193	5275	226	725	S243	4375	226
626	S144	6157	81	676	S194	5257	81	726	S244	4357	81
627	S145	6139	226	677	S195	5239	226	727	S245	4339	226
628	S146	6121	81	678	S196	5221	81	728	S246	4321	81
629	S147	6103	226	679	S197	5203	226	729	S247	4303	226
630	S148	6085	81	680	S198	5185	81	730	S248	4285	81
631	S149	6067	226	681	S199	5167	226	731	S249	4267	226
632	S150	6049	81	682	S200	5149	81	732	S250	4249	81
633	S151	6031	226	683	S201	5131	226	733	S251	4231	226
634	S152	6013	81	684	S202	5113	81	734	S252	4213	81
635	S153	5995	226	685	S203	5095	226	735	S253	4195	226
636	S154	5977	81	686	S204	5077	81	736	S254	4177	81
637	S155	5959	226	687	S205	5059	226	737	S255	4159	226
638	S156	5941	81	688	S206	5041	81	738	S256	4141	81
639	S157	5923	226	689	S207	5023	226	739	S257	4123	226
640	S158	5905	81	690	S208	5005	81	740	S258	4105	81
641	S159	5887	226	691	S209	4987	226	741	S259	4087	226
642	S160	5869	81	692	S210	4969	81	742	S260	4069	81
643	S161	5851	226	693	S211	4951	226	743	S261	4051	226
644	S162	5833	81	694	S212	4933	81	744	S262	4033	81
645	S163	5815	226	695	S213	4915	226	745	S263	4015	226
646	S164	5797	81	696	S214	4897	81	746	S264	3997	81
647	S165	5779	226	697	S215	4879	226	747	S265	3979	226
648	S166	5761	81	698	S216	4861	81	748	S266	3961	81
649	S167	5743	226	699	S217	4843	226	749	S267	3943	226
650	S168	5725	81	700	S218	4825	81	750	S268	3925	81

Pad #	Pad Name	X-pos	Y-pos	Pad #	Pad Name	X-pos	Y-pos	Pad #	Pad Name	X-pos	Y-pos
751	S269	3907	226	801	S319	3007	226	851	S369	2107	226
752	S270	3889	81	802	S320	2989	81	852	S370	2089	81
753	S271	3871	226	803	S321	2971	226	853	S371	2071	226
754	S272	3853	81	804	S322	2953	81	854	S372	2053	81
755	S273	3835	226	805	S323	2935	226	855	S373	2035	226
756	S274	3817	81	806	S324	2917	81	856	S374	2017	81
757	S275	3799	226	807	S325	2899	226	857	S375	1999	226
758	S276	3781	81	808	S326	2881	81	858	S376	1981	81
759	S277	3763	226	809	S327	2863	226	859	S377	1963	226
760	S278	3745	81	810	S328	2845	81	860	S378	1945	81
761	S279	3727	226	811	S329	2827	226	861	S379	1927	226
762	S280	3709	81	812	S330	2809	81	862	S380	1909	81
763	S281	3691	226	813	S331	2791	226	863	S381	1891	226
764	S282	3673	81	814	S332	2773	81	864	S382	1873	81
765	S283	3655	226	815	S333	2755	226	865	S383	1855	226
766	S284	3637	81	816	S334	2737	81	866	S384	1837	81
767	S285	3619	226	817	S335	2719	226	867	S385	1819	226
768	S286	3601	81	818	S336	2701	81	868	S386	1801	81
769	S287	3583	226	819	S337	2683	226	869	S387	1783	226
770	S288	3565	81	820	S338	2665	81	870	S388	1765	81
771	S289	3547	226	821	S339	2647	226	871	S389	1747	226
772	S290	3529	81	822	S340	2629	81	872	S390	1729	81
773	S291	3511	226	823	S341	2611	226	873	S391	1711	226
774	S292	3493	81	824	S342	2593	81	874	S392	1693	81
775	S293	3475	226	825	S343	2575	226	875	S393	1675	226
776	S294	3457	81	826	S344	2557	81	876	S394	1657	81
777	S295	3439	226	827	S345	2539	226	877	S395	1639	226
778	S296	3421	81	828	S346	2521	81	878	S396	1621	81
779	S297	3403	226	829	S347	2503	226	879	S397	1603	226
780	S298	3385	81	830	S348	2485	81	880	S398	1585	81
781	S299	3367	226	831	S349	2467	226	881	S399	1567	226
782	S300	3349	81	832	S350	2449	81	882	S400	1549	81
783	S301	3331	226	833	S351	2431	226	883	S401	1531	226
784	S302	3313	81	834	S352	2413	81	884	S402	1513	81
785	S303	3295	226	835	S353	2395	226	885	S403	1495	226
786	S304	3277	81	836	S354	2377	81	886	S404	1477	81
787	S305	3259	226	837	S355	2359	226	887	S405	1459	226
788	S306	3241	81	838	S356	2341	81	888	S406	1441	81
789	S307	3223	226	839	S357	2323	226	889	S407	1423	226
790	S308	3205	81	840	S358	2305	81	890	S408	1405	81
791	S309	3187	226	841	S359	2287	226	891	S409	1387	226
792	S310	3169	81	842	S360	2269	81	892	S410	1369	81
793	S311	3151	226	843	S361	2251	226	893	S411	1351	226
794	S312	3133	81	844	S362	2233	81	894	S412	1333	81
795	S313	3115	226	845	S363	2215	226	895	S413	1315	226
796	S314	3097	81	846	S364	2197	81	896	S414	1297	81
797	S315	3079	226	847	S365	2179	226	897	S415	1279	226
798	S316	3061	81	848	S366	2161	81	898	S416	1261	81
799	S317	3043	226	849	S367	2143	226	899	S417	1243	226
800	S318	3025	81	850	S368	2125	81	900	S418	1225	81

Pad #	Pad Name	X-pos	Y-pos	Pad #	Pad Name	X-pos	Y-pos	Pad #	Pad Name	X-pos	Y-pos
901	S419	1207	226	951	S469	307	226	1001	S509	-613	226
902	S420	1189	81	952	S470	289	81	1002	S510	-631	81
903	S421	1171	226	953	S471	271	226	1003	S511	-649	226
904	S422	1153	81	954	S472	253	81	1004	S512	-667	81
905	S423	1135	226	955	S473	235	226	1005	S513	-685	226
906	S424	1117	81	956	S474	217	81	1006	S514	-703	81
907	S425	1099	226	957	S475	199	226	1007	S515	-721	226
908	S426	1081	81	958	S476	181	81	1008	S516	-739	81
909	S427	1063	226	959	S477	163	226	1009	S517	-757	226
910	S428	1045	81	960	S478	145	81	1010	S518	-775	81
911	S429	1027	226	961	S479	127	226	1011	S519	-793	226
912	S430	1009	81	962	S480	109	81	1012	S520	-811	81
913	S431	991	226	963	DUMMY	91	226	1013	S521	-829	226
914	S432	973	81	964	DUMMY	73	81	1014	S522	-847	81
915	S433	955	226	965	DUMMY	55	226	1015	S523	-865	226
916	S434	937	81	966	DUMMY	37	81	1016	S524	-883	81
917	S435	919	226	967	DUMMY	19	226	1017	S525	-901	226
918	S436	901	81	968	DUMMY	-19	81	1018	S526	-919	81
919	S437	883	226	969	DUMMY	-37	226	1019	S527	-937	226
920	S438	865	81	970	DUMMY	-55	81	1020	S528	-955	81
921	S439	847	226	971	DUMMY	-73	226	1021	S529	-973	226
922	S440	829	81	972	DUMMY	-91	81	1022	S530	-991	81
923	S441	811	226	973	S481	-109	226	1023	S531	-1009	226
924	S442	793	81	974	S482	-127	81	1024	S532	-1027	81
925	S443	775	226	975	S483	-145	226	1025	S533	-1045	226
926	S444	757	81	976	S484	-163	81	1026	S534	-1063	81
927	S445	739	226	977	S485	-181	226	1027	S535	-1081	226
928	S446	721	81	978	S486	-199	81	1028	S536	-1099	81
929	S447	703	226	979	S487	-217	226	1029	S537	-1117	226
930	S448	685	81	980	S488	-235	81	1030	S538	-1135	81
931	S449	667	226	981	S489	-253	226	1031	S539	-1153	226
932	S450	649	81	982	S490	-271	81	1032	S540	-1171	81
933	S451	631	226	983	S491	-289	226	1033	S541	-1189	226
934	S452	613	81	984	S492	-307	81	1034	S542	-1207	81
935	S453	595	226	985	S493	-325	226	1035	S543	-1225	226
936	S454	577	81	986	S494	-343	81	1036	S544	-1243	81
937	S455	559	226	987	S495	-361	226	1037	S545	-1261	226
938	S456	541	81	988	S496	-379	81	1038	S546	-1279	81
939	S457	523	226	989	S497	-397	226	1039	S547	-1297	226
940	S458	505	81	990	S498	-415	81	1040	S548	-1315	81
941	S459	487	226	991	S499	-433	226	1041	S549	-1333	226
942	S460	469	81	992	S500	-451	81	1042	S550	-1351	81
943	S461	451	226	993	S501	-469	226	1043	S551	-1369	226
944	S462	433	81	994	S502	-487	81	1044	S552	-1387	81
945	S463	415	226	995	S503	-505	226	1045	S553	-1405	226
946	S464	397	81	996	S504	-523	81	1046	S554	-1423	81
947	S465	379	226	997	S505	-541	226	1047	S555	-1441	226
948	S466	361	81	998	S506	-559	81	1048	S556	-1459	81
949	S467	343	226	999	S507	-577	226	1049	S557	-1477	226
950	S468	325	81	1000	S508	-595	81	1050	S558	-1495	81

Pad #	Pad Name	X-pos	Y-pos	Pad #	Pad Name	X-pos	Y-pos	Pad #	Pad Name	X-pos	Y-pos
1051	S559	-1513	226	1101	S609	-2413	226	1151	S659	-3313	226
1052	S560	-1531	81	1102	S610	-2431	81	1152	S660	-3331	81
1053	S561	-1549	226	1103	S611	-2449	226	1153	S661	-3349	226
1054	S562	-1567	81	1104	S612	-2467	81	1154	S662	-3367	81
1055	S563	-1585	226	1105	S613	-2485	226	1155	S663	-3385	226
1056	S564	-1603	81	1106	S614	-2503	81	1156	S664	-3403	81
1057	S565	-1621	226	1107	S615	-2521	226	1157	S665	-3421	226
1058	S566	-1639	81	1108	S616	-2539	81	1158	S666	-3439	81
1059	S567	-1657	226	1109	S617	-2557	226	1159	S667	-3457	226
1060	S568	-1675	81	1110	S618	-2575	81	1160	S668	-3475	81
1061	S569	-1693	226	1111	S619	-2593	226	1161	S669	-3493	226
1062	S570	-1711	81	1112	S620	-2611	81	1162	S670	-3511	81
1063	S571	-1729	226	1113	S621	-2629	226	1163	S671	-3529	226
1064	S572	-1747	81	1114	S622	-2647	81	1164	S672	-3547	81
1065	S573	-1765	226	1115	S623	-2665	226	1165	S673	-3565	226
1066	S574	-1783	81	1116	S624	-2683	81	1166	S674	-3583	81
1067	S575	-1801	226	1117	S625	-2701	226	1167	S675	-3601	226
1068	S576	-1819	81	1118	S626	-2719	81	1168	S676	-3619	81
1069	S577	-1837	226	1119	S627	-2737	226	1169	S677	-3637	226
1070	S578	-1855	81	1120	S628	-2755	81	1170	S678	-3655	81
1071	S579	-1873	226	1121	S629	-2773	226	1171	S679	-3673	226
1072	S580	-1891	81	1122	S630	-2791	81	1172	S680	-3691	81
1073	S581	-1909	226	1123	S631	-2809	226	1173	S681	-3709	226
1074	S582	-1927	81	1124	S632	-2827	81	1174	S682	-3727	81
1075	S583	-1945	226	1125	S633	-2845	226	1175	S683	-3745	226
1076	S584	-1963	81	1126	S634	-2863	81	1176	S684	-3763	81
1077	S585	-1981	226	1127	S635	-2881	226	1177	S685	-3781	226
1078	S586	-1999	81	1128	S636	-2899	81	1178	S686	-3799	81
1079	S587	-2017	226	1129	S637	-2917	226	1179	S687	-3817	226
1080	S588	-2035	81	1130	S638	-2935	81	1180	S688	-3835	81
1081	S589	-2053	226	1131	S639	-2953	226	1181	S689	-3853	226
1082	S590	-2071	81	1132	S640	-2971	81	1182	S690	-3871	81
1083	S591	-2089	226	1133	S641	-2989	226	1183	S691	-3889	226
1084	S592	-2107	81	1134	S642	-3007	81	1184	S692	-3907	81
1085	S593	-2125	226	1135	S643	-3025	226	1185	S693	-3925	226
1086	S594	-2143	81	1136	S644	-3043	81	1186	S694	-3943	81
1087	S595	-2161	226	1137	S645	-3061	226	1187	S695	-3961	226
1088	S596	-2179	81	1138	S646	-3079	81	1188	S696	-3979	81
1089	S597	-2197	226	1139	S647	-3097	226	1189	S697	-3997	226
1090	S598	-2215	81	1140	S648	-3115	81	1190	S698	-4015	81
1091	S599	-2233	226	1141	S649	-3133	226	1191	S699	-4033	226
1092	S600	-2251	81	1142	S650	-3151	81	1192	S700	-4051	81
1093	S601	-2269	226	1143	S651	-3169	226	1193	S701	-4069	226
1094	S602	-2287	81	1144	S652	-3187	81	1194	S702	-4087	81
1095	S603	-2305	226	1145	S653	-3205	226	1195	S703	-4105	226
1096	S604	-2323	81	1146	S654	-3223	81	1196	S704	-4123	81
1097	S605	-2341	226	1147	S655	-3241	226	1197	S705	-4141	226
1098	S606	-2359	81	1148	S656	-3259	81	1198	S706	-4159	81
1099	S607	-2377	226	1149	S657	-3277	226	1199	S707	-4177	226
1100	S608	-2395	81	1150	S658	-3295	81	1200	S708	-4195	81

Pad #	Pad Name	X-pos	Y-pos	Pad #	Pad Name	X-pos	Y-pos	Pad #	Pad Name	X-pos	Y-pos
1201	S709	-4213	226	1251	S759	-5113	226	1301	S809	-6013	226
1202	S710	-4231	81	1252	S760	-5131	81	1302	S810	-6031	81
1203	S711	-4249	226	1253	S761	-5149	226	1303	S811	-6049	226
1204	S712	-4267	81	1254	S762	-5167	81	1304	S812	-6067	81
1205	S713	-4285	226	1255	S763	-5185	226	1305	S813	-6085	226
1206	S714	-4303	81	1256	S764	-5203	81	1306	S814	-6103	81
1207	S715	-4321	226	1257	S765	-5221	226	1307	S815	-6121	226
1208	S716	-4339	81	1258	S766	-5239	81	1308	S816	-6139	81
1209	S717	-4357	226	1259	S767	-5257	226	1309	S817	-6157	226
1210	S718	-4375	81	1260	S768	-5275	81	1310	S818	-6175	81
1211	S719	-4393	226	1261	S769	-5293	226	1311	S819	-6193	226
1212	S720	-4411	81	1262	S770	-5311	81	1312	S820	-6211	81
1213	S721	-4429	226	1263	S771	-5329	226	1313	S821	-6229	226
1214	S722	-4447	81	1264	S772	-5347	81	1314	S822	-6247	81
1215	S723	-4465	226	1265	S773	-5365	226	1315	S823	-6265	226
1216	S724	-4483	81	1266	S774	-5383	81	1316	S824	-6283	81
1217	S725	-4501	226	1267	S775	-5401	226	1317	S825	-6301	226
1218	S726	-4519	81	1268	S776	-5419	81	1318	S826	-6319	81
1219	S727	-4537	226	1269	S777	-5437	226	1319	S827	-6337	226
1220	S728	-4555	81	1270	S778	-5455	81	1320	S828	-6355	81
1221	S729	-4573	226	1271	S779	-5473	226	1321	S829	-6373	226
1222	S730	-4591	81	1272	S780	-5491	81	1322	S830	-6391	81
1223	S731	-4609	226	1273	S781	-5509	226	1323	S831	-6409	226
1224	S732	-4627	81	1274	S782	-5527	81	1324	S832	-6427	81
1225	S733	-4645	226	1275	S783	-5545	226	1325	S833	-6445	226
1226	S734	-4663	81	1276	S784	-5563	81	1326	S834	-6463	81
1227	S735	-4681	226	1277	S785	-5581	226	1327	S835	-6481	226
1228	S736	-4699	81	1278	S786	-5599	81	1328	S836	-6499	81
1229	S737	-4717	226	1279	S787	-5617	226	1329	S837	-6517	226
1230	S738	-4735	81	1280	S788	-5635	81	1330	S838	-6535	81
1231	S739	-4753	226	1281	S789	-5653	226	1331	S839	-6553	226
1232	S740	-4771	81	1282	S790	-5671	81	1332	S840	-6571	81
1233	S741	-4789	226	1283	S791	-5689	226	1333	S841	-6589	226
1234	S742	-4807	81	1284	S792	-5707	81	1334	S842	-6607	81
1235	S743	-4825	226	1285	S793	-5725	226	1335	S843	-6625	226
1236	S744	-4843	81	1286	S794	-5743	81	1336	S844	-6643	81
1237	S745	-4861	226	1287	S795	-5761	226	1337	S845	-6661	226
1238	S746	-4879	81	1288	S796	-5779	81	1338	S846	-6679	81
1239	S747	-4897	226	1289	S797	-5797	226	1339	S847	-6697	226
1240	S748	-4915	81	1290	S798	-5815	81	1340	S848	-6715	81
1241	S749	-4933	226	1291	S799	-5833	226	1341	S849	-6733	226
1242	S750	-4951	81	1292	S800	-5851	81	1342	S850	-6751	81
1243	S751	-4969	226	1293	S801	-5869	226	1343	S851	-6769	226
1244	S752	-4987	81	1294	S802	-5887	81	1344	S852	-6787	81
1245	S753	-5005	226	1295	S803	-5905	226	1345	S853	-6805	226
1246	S754	-5023	81	1296	S804	-5923	81	1346	S854	-6823	81
1247	S755	-5041	226	1297	S805	-5941	226	1347	S855	-6841	226
1248	S756	-5059	81	1298	S806	-5959	81	1348	S856	-6859	81
1249	S757	-5077	226	1299	S807	-5977	226	1349	S857	-6877	226
1250	S758	-5095	81	1300	S808	-5995	81	1350	S858	-6895	81

Pad #	Pad Name	X-pos	Y-pos	Pad #	Pad Name	X-pos	Y-pos	Pad #	Pad Name	X-pos	Y-pos
1351	S859	-6913	226	1401	S909	-7813	226	1451	S959	-8713	226
1352	S860	-6931	81	1402	S910	-7831	81	1452	S960	-8731	81
1353	S861	-6949	226	1403	S911	-7849	226	1453	DUMMY	-8763	226
1354	S862	-6967	81	1404	S912	-7867	81	1454	DUMMY	-8781	81
1355	S863	-6985	226	1405	S913	-7885	226	1455	G240	-8799	226
1356	S864	-7003	81	1406	S914	-7903	81	1456	G238	-8817	81
1357	S865	-7021	226	1407	S915	-7921	226	1457	G236	-8835	226
1358	S866	-7039	81	1408	S916	-7939	81	1458	G234	-8853	81
1359	S867	-7057	226	1409	S917	-7957	226	1459	G232	-8871	226
1360	S868	-7075	81	1410	S918	-7975	81	1460	G230	-8889	81
1361	S869	-7093	226	1411	S919	-7993	226	1461	G228	-8907	226
1362	S870	-7111	81	1412	S920	-8011	81	1462	G226	-8925	81
1363	S871	-7129	226	1413	S921	-8029	226	1463	G224	-8943	226
1364	S872	-7147	81	1414	S922	-8047	81	1464	G222	-8961	81
1365	S873	-7165	226	1415	S923	-8065	226	1465	G220	-8979	226
1366	S874	-7183	81	1416	S924	-8083	81	1466	G218	-8997	81
1367	S875	-7201	226	1417	S925	-8101	226	1467	G216	-9015	226
1368	S876	-7219	81	1418	S926	-8119	81	1468	G214	-9033	81
1369	S877	-7237	226	1419	S927	-8137	226	1469	G212	-9051	226
1370	S878	-7255	81	1420	S928	-8155	81	1470	G210	-9069	81
1371	S879	-7273	226	1421	S929	-8173	226	1471	G208	-9087	226
1372	S880	-7291	81	1422	S930	-8191	81	1472	G206	-9105	81
1373	S881	-7309	226	1423	S931	-8209	226	1473	G204	-9123	226
1374	S882	-7327	81	1424	S932	-8227	81	1474	G202	-9141	81
1375	S883	-7345	226	1425	S933	-8245	226	1475	G200	-9159	226
1376	S884	-7363	81	1426	S934	-8263	81	1476	G198	-9177	81
1377	S885	-7381	226	1427	S935	-8281	226	1477	G196	-9195	226
1378	S886	-7399	81	1428	S936	-8299	81	1478	G194	-9213	81
1379	S887	-7417	226	1429	S937	-8317	226	1479	G192	-9231	226
1380	S888	-7435	81	1430	S938	-8335	81	1480	G190	-9249	81
1381	S889	-7453	226	1431	S939	-8353	226	1481	G188	-9267	226
1382	S890	-7471	81	1432	S940	-8371	81	1482	G186	-9285	81
1383	S891	-7489	226	1433	S941	-8389	226	1483	G184	-9303	226
1384	S892	-7507	81	1434	S942	-8407	81	1484	G182	-9321	81
1385	S893	-7525	226	1435	S943	-8425	226	1485	G180	-9339	226
1386	S894	-7543	81	1436	S944	-8443	81	1486	G178	-9357	81
1387	S895	-7561	226	1437	S945	-8461	226	1487	G176	-9375	226
1388	S896	-7579	81	1438	S946	-8479	81	1488	G174	-9393	81
1389	S897	-7597	226	1439	S947	-8497	226	1489	G172	-9411	226
1390	S898	-7615	81	1440	S948	-8515	81	1490	G170	-9429	81
1391	S899	-7633	226	1441	S949	-8533	226	1491	G168	-9447	226
1392	S900	-7651	81	1442	S950	-8551	81	1492	G166	-9465	81
1393	S901	-7669	226	1443	S951	-8569	226	1493	G164	-9483	226
1394	S902	-7687	81	1444	S952	-8587	81	1494	G162	-9501	81
1395	S903	-7705	226	1445	S953	-8605	226	1495	G160	-9519	226
1396	S904	-7723	81	1446	S954	-8623	81	1496	G158	-9537	81
1397	S905	-7741	226	1447	S955	-8641	226	1497	G156	-9555	226
1398	S906	-7759	81	1448	S956	-8659	81	1498	G154	-9573	81
1399	S907	-7777	226	1449	S957	-8677	226	1499	G152	-9591	226
1400	S908	-7795	81	1450	S958	-8695	81	1500	G150	-9609	81

Pad #	Pad Name	X-pos	Y-pos	Pad #	Pad Name	X-pos	Y-pos
1501	G148	-9627	226	1551	G48	-10527	226
1502	G146	-9645	81	1552	G46	-10545	81
1503	G144	-9663	226	1553	G44	-10563	226
1504	G142	-9681	81	1554	G42	-10581	81
1505	G140	-9699	226	1555	G40	-10599	226
1506	G138	-9717	81	1556	G38	-10617	81
1507	G136	-9735	226	1557	G36	-10635	226
1508	G134	-9753	81	1558	G34	-10653	81
1509	G132	-9771	226	1559	G32	-10671	226
1510	G130	-9789	81	1560	G30	-10689	81
1511	G128	-9807	226	1561	G28	-10707	226
1512	G126	-9825	81	1562	G26	-10725	81
1513	G124	-9843	226	1563	G24	-10743	226
1514	G122	-9861	81	1564	G22	-10761	81
1515	G120	-9879	226	1565	G20	-10779	226
1516	G118	-9897	81	1566	G18	-10797	81
1517	G116	-9915	226	1567	G16	-10815	226
1518	G114	-9933	81	1568	G14	-10833	81
1519	G112	-9951	226	1569	G12	-10851	226
1520	G110	-9969	81	1570	G10	-10869	81
1521	G108	-9987	226	1571	G8	-10887	226
1522	G106	-10005	81	1572	G6	-10905	81
1523	G104	-10023	226	1573	G4	-10923	226
1524	G102	-10041	81	1574	G2	-10941	81
1525	G100	-10059	226				
1526	G98	-10077	81				
1527	G96	-10095	226				
1528	G94	-10113	81				
1529	G92	-10131	226				
1530	G90	-10149	81				
1531	G88	-10167	226				
1532	G86	-10185	81				
1533	G84	-10203	226				
1534	G82	-10221	81				
1535	G80	-10239	226				
1536	G78	-10257	81				
1537	G76	-10275	226				
1538	G74	-10293	81				
1539	G72	-10311	226				
1540	G70	-10329	81				
1541	G68	-10347	226				
1542	G66	-10365	81				
1543	G64	-10383	226				
1544	G62	-10401	81				
1545	G60	-10419	226				
1546	G58	-10437	81				
1547	G56	-10455	226				
1548	G54	-10473	81				
1549	G52	-10491	226				
1550	G50	-10509	81				

6 PIN DESCRIPTION

Remark:

I = Input;
O = Output;
IO = Bi-directional;
P = Power;,
GND = System VSS;

Table 6-1: Power Supply Pins

Pin Name	Type	Connect to	Function	Description	When not in use
VSS	P	GND	Ground of the Power Supply	System ground pin of the IC.	-
VSSRC		GND		Grounding for gamma circuit	-
AVSS		GND		Grounding for analog circuit.	-
VCHS		AVSS		Grounding for booster circuit.	-
VCI	P	Power Supply	Power Supply for Analog Circuits	Booster input voltage pin. - Connect to voltage source between 2.5V to 3.6V	-
VCIP		VCI		Voltage supply pin for analog circuit. This pin requires a noise free path for providing accurate LCD driving voltages. - Connect to same source of VCI	-
VCIM	O	Stabilizing capacitor	Booster voltages	Negative voltage of VCI.	-
VCIX2		Stabilizing capacitor		Equals to 2x VCI	-
VCIX2G		VCIX2 on FPC			-
VCOMR	I	External voltage source or Open	External Reference	This pin provides voltage reference for internal voltage regulator when register VDV[4:0] of Power Control 4 set to "01111". - Connect to an external voltage source for reference	Open
VCOMH	O	Stabilizing capacitor	Voltages for VCOM Signal	This pin indicates a HIGH level of VCOM generated in driving the VCOM alternation.	-
VCOML		Stabilizing capacitor		This pin indicates a LOW level of VCOM generated in driving the VCOM alternation.	-
VLCD63	O	Stabilizing capacitor	LCD Driving Voltages	This pin is the maximum source driver voltage.	-
VGH		Stabilizing capacitor		A positive power output pin for gate driver and for OTP programming	-
VGL		Stabilizing capacitor		A negative power output pin for gate driver.	-
EXVR	I	GND	External Reference	External reference of internal gamma resistor - Connect to VSS	-
CXP	I	Booster capacitor	Booster and Stabilization Capacitors	- Connect a capacitor to CXN	-
CXN				- Connect a capacitor to CXP	-
CYP		Booster capacitor		- Connect a capacitor to CYN	-
CYN				- Connect a capacitor to CYP	-
C1P		Booster capacitor		- Connect a capacitor to C1N	-
C1N				- Connect a capacitor to C1P	-
C2P		Booster capacitor		- Connect a capacitor to C2N	-
C2N				- Connect a capacitor to C2P	-
C3P		Booster capacitor		- Connect a capacitor to C3N	-
C3N				- Connect a capacitor to C3P	-

Pin Name	Type	Connect to	Function	Description	When not in use
CDUM0		Stabilizing capacitor	Stabilizing capacitor	- Connect a capacitor to VSS	Open
VCORE	P	Stabilizing capacitor	Power for Core Logic	Vdd for core use. Connect a capacitor for stabilization	-
VREGC	P	VCORE	Regulator output for logic circuits	Regulator output for VCORE use.	-
VDDIO	P	Power Supply	Power for interface logic pins	Voltage input pin for logic I/O, connect to system VDD. - Connect to voltage source between 1.4V to 3.6V	-

Table 6-2: Interface Logic Pins

Name	Type	Connect to	Function	Description	When not in use
DC/SDC	I	MPU	Logic Control	Data or command **DC** : Parallel Interface **SDC** : Serial Interface	V_{DDIO} or V_{ss}
CS/SCS		MPU		**CS** : Chip select pin for 6800/8080 Parallel Interface **SCS** : Chip Select pin for Serial Mode Interface	-
RD		MPU		6800-system : **E** (enable signal) 8080-system : **RD** (read strobe signal) Serial mode : Not used and should be connected to V_{DDIO} or V_{ss}	V_{DDIO} or V_{ss}
RW		MPU		6800-system : **RW** (indicates read cycle when High, write cycle when Low) 8080-system : **WR** (write strobe signal)	V_{DDIO} or V_{ss}
D0-D17	IO	MPU	Data bus	For parallel mode, 8/9/16/18 bit interface. Please refer to Section 15 Interface Mapping Section for definition. Unused pins should connect to V_{SS}.	V_{SS}
WSYNC	O	MPU	Display Timing Signal	Ram Write Synchronization output	Open
DOTCLK	I	MPU		Dot-clock signal and oscillator source. A non-stop external clock must be provided to that pin even at front or black porch non-display period.	Vss
HSYNC	I	MPU		Line Synchronization input	V_{SS}
VSYNC	I	MPU		Frame/Ram Write Synchronization input	V_{SS}
DEN	I	MPU		Display enable pin from controller.	Vss
RESB	I	MPU	System Reset	System reset pin. - An active low pulse at this pin will reset the IC, Connect to V_{DDIO} in normal operation An external reset pulse to RESB is required for power up (sequence)	-
SDI	I	MPU	Serial interface	Data input pin in serial interface	V_{SS}
SDO	O	MPU		Data output pin in serial interface	Open
SCL	I	MPU		Serial clock input	Vss

Table 6-3: Mode Selection Pins

Name	Type	Connect to	Function	Description	When not in use
PS[3:0]	I	V_{DDIO} or V_{SS}	Interface Selection	See below	-

PS3	PS2	PS1	PS0	Interface Mode
0	0	0	0	16-bit 6800 parallel interface
0	0	0	1	8-bit 6800 parallel interface
0	0	1	0	16-bit 8080 parallel interface
0	0	1	1	8-bit 8080 parallel interface
0	1	0	0	9-bit generic D[17:9] (262k colour) + 3-wire SPI If 65K color, D12 shorts to D17 internally
0	1	0	1	16-bit generic (262k colour) + 3-wire SPI
0	1	1	0	18-bit generic (262k colour) + 3-wire SPI
0	1	1	1	6-bit generic D[17:12] (262k colour) + 3-wire SPI
1	0	0	0	18-bits 6800 parallel interface
1	0	0	1	9-bits 6800 parallel interface
1	0	1	0	18-bit 8080 parallel interface
1	0	1	1	9-bit 8080 parallel interface
1	1	1	0	3-wire SPI
1	1	1	1	4-wire SPI

Table 6-4: Driver Output Pins

Name	Type	Connect to	Function	Description	When not in use
VCOM	O	LCD	LCD Driving Signals	A power supply for the TFT-display common electrode.	Open
G1-G240		LCD		Gate driver output pins. These pins output V_{GH}, V_{GL} or V_{GOFFH} level.	Open
S1-S960		LCD		Source driver output pins. S(3n+1) : display Red if BGR = LOW, Blue if BGR = HIGH. S(3n+2) : display Green. S(3n) : display Blue if BGR = LOW, Red if BGR = HIGH.	Open

Table 6-5: Miscellaneous Pins

Name	Type	Connect to	Function	Description	When not in use
NC	-	-	-	These pins must be left open and cannot be connected together	Open
DUMMY		-		Floating pins and no connection inside the IC. These pins should be open.	Open

7 FUNCTION BLOCK DESCRIPTIONS

7.1 System Interface

The System Interface unit consists of three functional blocks for driving the 6800-series parallel interface, 8080-series high speed parallel interface, 3-lines serial peripheral interface and 4-lines serial peripheral interface. The selection of different interface is done by PS3, PS2, PS1 and PS0 pins. Please refer to the pin descriptions on page 13 and 13.

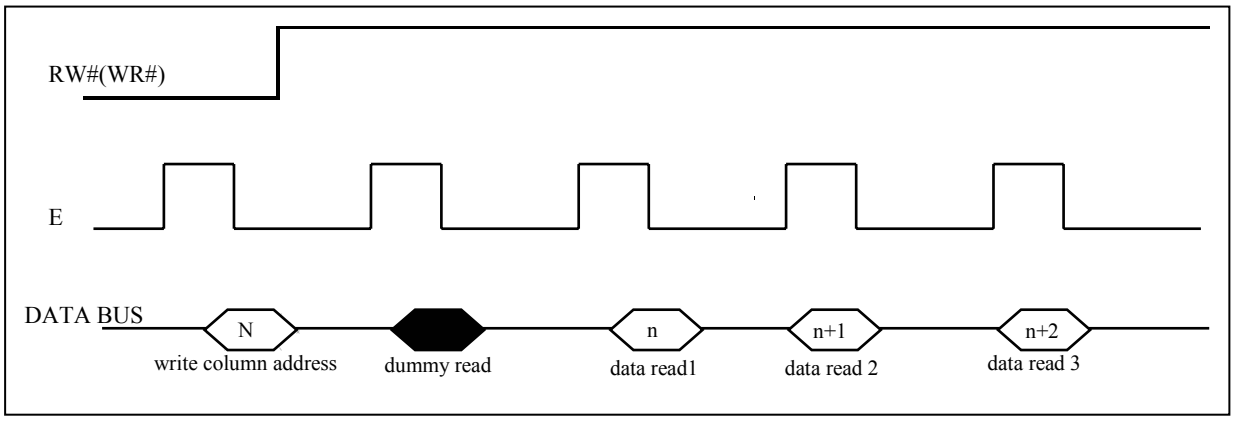
Table 7-1: Data bus selection modes

	6800 – series Parallel Interface	8080 – series Parallel Interface	MCU Serial Interface
Data Read	18/16/9/8-bits	18/16/9/8-bits	Yes
Data Write	18/16/9/8-bits	18/16/9/8-bits	8-bits
Command Read	Status only	Status only	No
Command Write	Yes	Yes	8-bits

7.1.1 MPU Parallel 6800-series Interface

The parallel Interface consists of 18 bi-directional data pins D[17:0], RW, DC, E and CS.
RW input high indicates a read operation from the Graphical Display Data RAM (GDDRAM) or status register. RW input low indicates a write operation to Display Data RAM or Internal Command Registers depending on the status of DC input.
The E input served as data latch signal (clock) when high provided that CS is low. Please refer to Parallel Interface Timing Diagram of 6800-series microprocessors.
In order to match the operating frequency of the GDDRAM with that of the MCU, pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in the following diagram.

Figure 7-1: Read Display Data



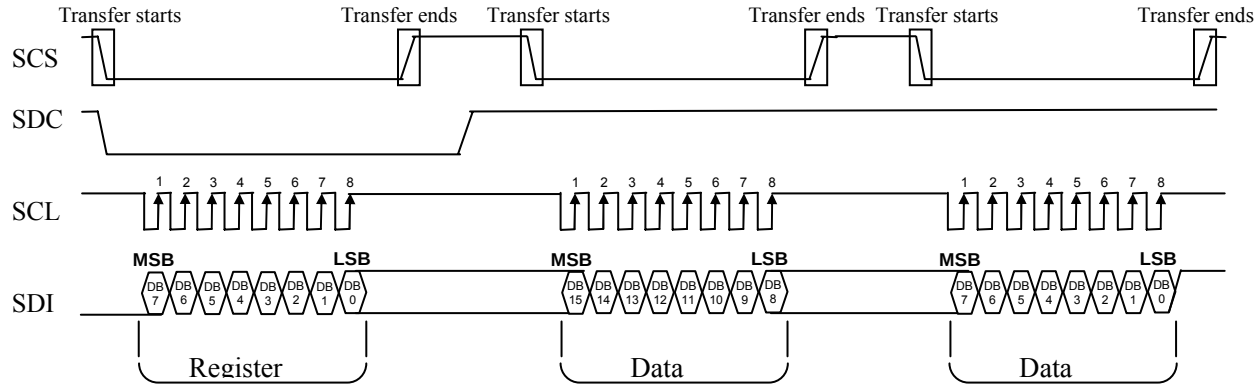
7.1.2 MPU Parallel 8080-series Interface

The parallel interface consists of 18 bi-directional data pins D[17:0], WR, DC, and CS.
RD input served as data read latch signal (clock) when low provided that CS is low. Weather reading the display data from GDDRAM or reading the status from the status register is controlled by DC. WR input served as data write latch signal (clock) when low provided that CS is low. Weather writing the display data to the GDDRAM or writing the command to the command register is controlled by DC. A dummy read is also required before the first actual display data read for 8080-series interface. Please refer to .

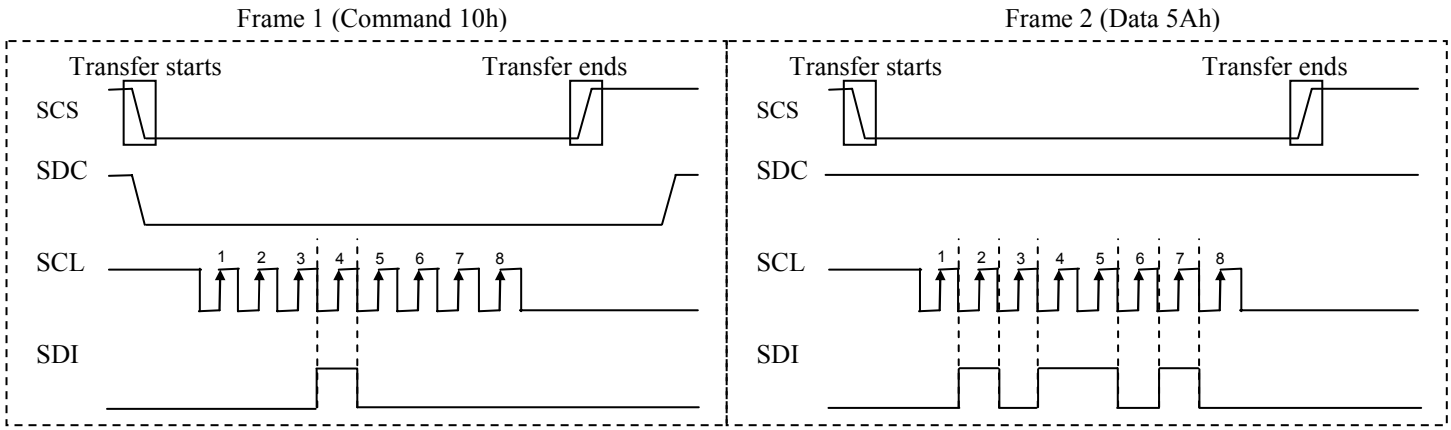
7.1.3 4-wire Serial Peripheral Interface (8 bits)

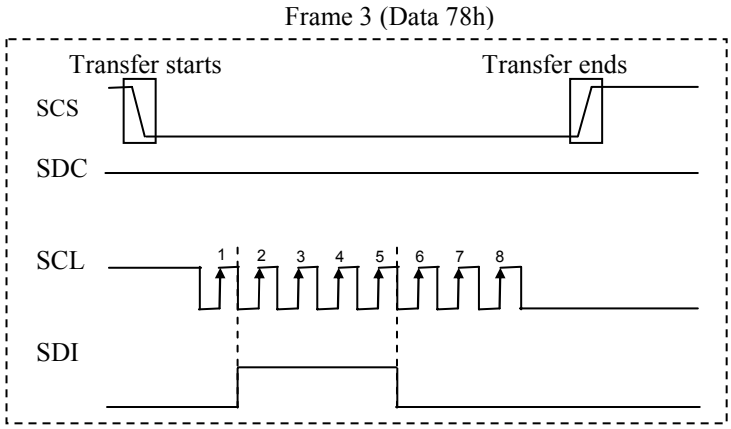
The clock synchronized serial peripheral interface (SPI) using the chip select line (SCS), serial transfer clock line (SCL), serial input data (SDI). The serial data transfer starts at the falling edge of SCS input and ends at the rising edge of SCS.
SDC determinates the data of SDI which is register or data.

Figure 7-2: 4-wire SPI interface (8 bits)



Example of 4-wires (8 bits)

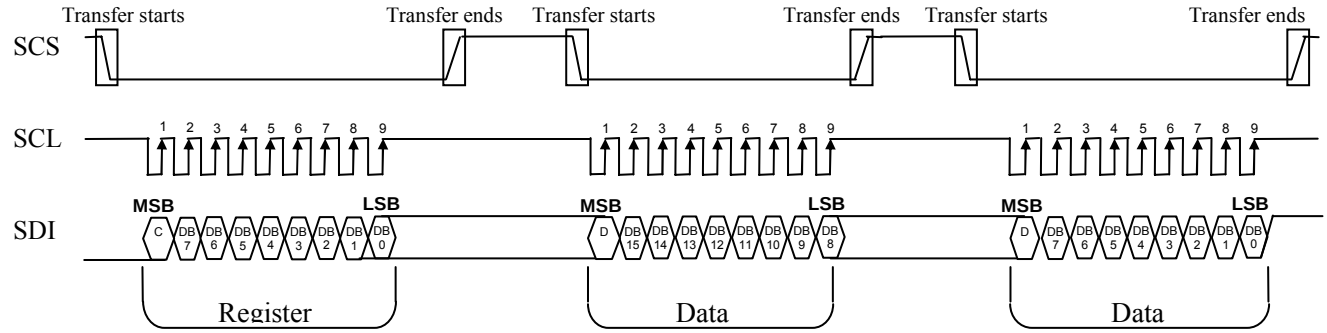




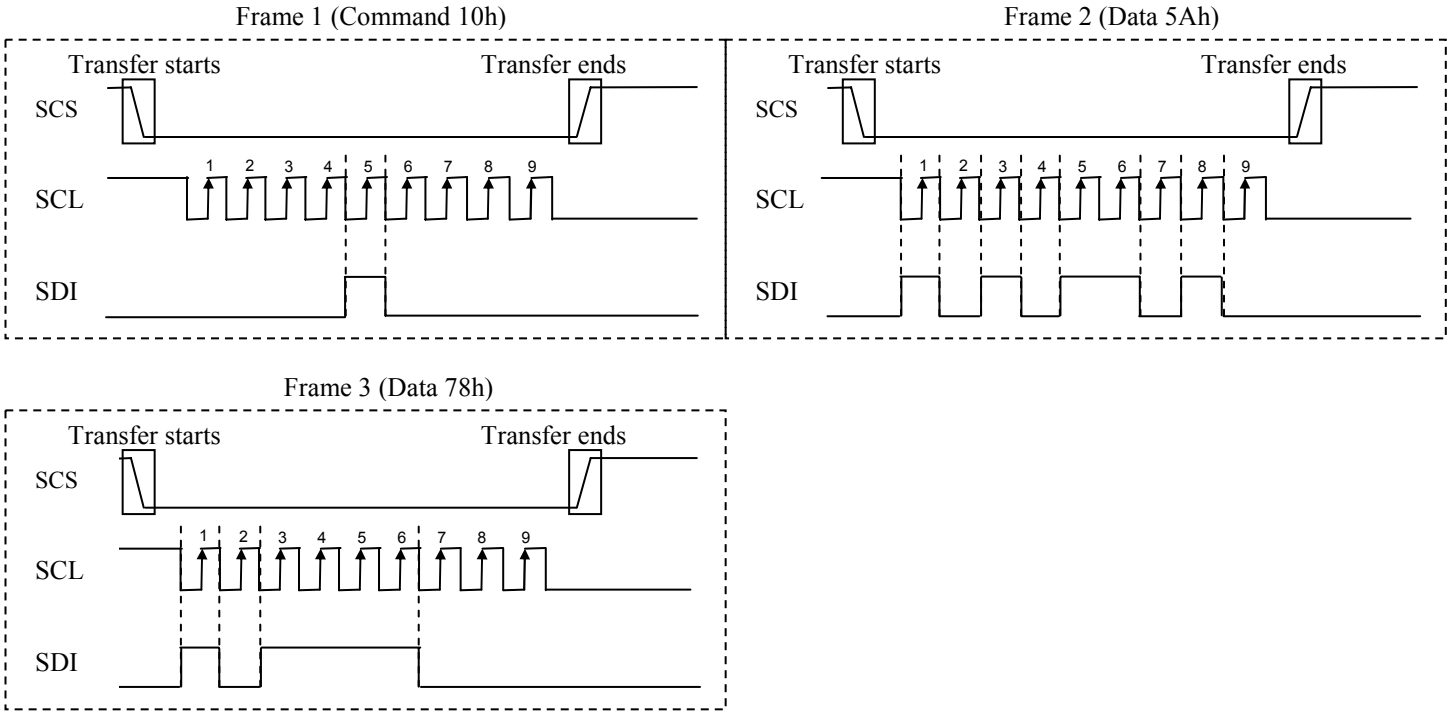
7.1.4 3-lines Serial Peripheral Interface

The operation is similar to 4-lines serial peripheral interface while SDC is not use. There are altogether 9-bits will be shifted into the shift register on every ninth clock in sequence: DC bit, D7 to D0 bit. The DC bit (first bit of the sequential data) will determine the following data byte in the shift register is written to the Display Data RAM (DC bit = 1) or the command register (DC bit = 0).

Figure 7-3: 3-wire SPI interface (9 bits)



Example of 3-wires (9 bits)



7.2 RGB Interface

SSD2119 supports RGB interface. RGB interface unit consists of D[17:0], HSYNC, VSYNC, DOTCLK and DEN signals for display moving pictures. When the RGB interface is selected, the display operation is synchronized with external control signals (HSYNC, VSYNC and DOTCLK). Data is written in synchronization with the control signals when DEN is enabled for write operation in order to avoid flicker or tearing effect while updating display data.

7.3 Address Counter (AC)

The address counter (AC) assigns address to the GDDRAM. When an address set instruction is written into the IR, the address information is sent from the IR to the AC.

After writing into the GRAM, the AC is automatically incremented by 1 (or decremented by 1). After reading the data, the AC is not updated. A window address function allows for data to be written only to a window area specified by GRAM.

7.4 Graphic Display Data RAM (GDDRAM)

The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 320 RGB x 240 x 18 / 8 = 172,800 bytes. For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software. Please refer to the command "Data Output/Scan direction" for detail description.

Four pages of display data forms a RAM address block and stored in the GDDRAM. Each block will form the fundamental units of scrolling addresses. Various types of area scrolling can be performed by software program according to the command "Set area Scroll" and "Set Scroll Start".

7.5 Gamma/Grayscale Voltage Generator

The grayscale voltage circuit generates a LCD driver circuit that corresponds to the grayscale levels as specified in the grayscale gamma adjustment resister. 262,144 possible colors can be displayed when 1 pixel = 18 bit. For details, see the gamma adjustment register.

7.6 Booster and Regulator Circuit

These two functional blocks generate the voltage of VGH, VGL, VCOM levels and VLCD0~63 which are necessary for operating a TFT LCD.

7.7 Timing Generator

The timing generator generates a timing signal for the operation of internal circuit such as the internal RAM accessing, date output timing etc.

7.8 Oscillation Circuit (OSC)

This module is an on-chip low power RC oscillator circuitry. The oscillator generates the clock for the DC-DC voltage converter. This clock is also used in the display timing generator.

7.9 Data Latches

This block is a series of latches carrying the display signal information. These latches hold the data, which will be fed to the HV Buffer Cell and Level Selector to output the required voltage level.

7.10 Liquid Crystal Driver Circuit

SSD2119 consists of a 960-output source driver (S1-S960) and a 240-output gate driver (G1-G240). The display image data is latched when 960 bits of data are inputted. The latched data control the source driver and output drive waveforms. The gate driver for scanning gate lines outputs either VGH or VGL level. The shift direction of 960-bit source output from the source driver can be changed by setting the RL bit and the shift direction of gate output from the gate driver can be changed by setting the TB bit. The scan mode by the gate driver can be changed by setting the SM bit. Sets the gate driver pin arrangement in combination with the TB bit to select the optimal scan mode for the module.

8 COMMAND TABLE (TBC)

Table 8-1: Command Table

Reg#	Register	R/W	D/C	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R	Index	0	0	0	0	0	0	0	0	0	0	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
R00h	Oscillation Start	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	OSCEN
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R01h	Driver output control	0	1	0	RL	REV	GD	BGR	SM	TB	0	MUX7	MUX6	MUX5	MUX4	MUX3	MUX2	MUX1	MUX0
	(3AEFh)			0	0	1	1	1	0	1	0	1	1	1	0	1	1	1	1
R02h	LCD drive AC control	0	1	0	0	0	FLD	ENWS	B/C	EOR	WSMD	NW7	NW6	NW5	NW4	NW3	NW2	NW1	NW0
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R03h	Power control (1)	0	1	DCT3	DCT2	DCT1	DCT0	BT2	BT1	BT0	0	DC3	DC2	DC1	DC0	AP2	AP1	AP0	0
	All GAMAS[2:0] setting 8 color (6A64h)			0	1	1	0	1	0	1	0	0	1	1	0	0	1	0	0
R07h	Display control	0	1	0	0	0	PT1	PT0	VLE2	VLE1	SPT	0	0	GON	DTE	CM	0	D1	D0
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R0Bh	Frame cycle control	0	1	NO1	NO0	SDT1	SDT0	0	EQ2	EQ1	EQ0	DIV1	DIV0	SDIV	SRTN	RTN3	RTN2	RTN1	RTN0
	(5308h)			0	1	0	1	0	0	1	1	0	0	0	0	1	0	0	0
R0Ch	Power control (2)	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	VRC2	VRC1	VRC0
	(0004h)			0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
R0Dh	Power control (3)	0	1	0	0	0	0	0	0	0	0	0	0	0	0	VRH3	VRH2	VRH1	VRH0
R0Eh	Power control (4)	0	1	0	0	VCOMG	VDV4	VDV3	VDV2	VDV1	VDV0	0	0	0	0	0	0	0	0
R0Fh	Gate scan start position	0	1	0	0	0	0	0	0	0	SCN8	SCN7	SCN6	SCN5	SCN4	SCN3	SCN2	SCN1	SCN0
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R10h	Sleep mode	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SLP
	(0001h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R11h	Entry mode	0	1	VS mode	DFM1	DFM0	0	Denmode	WMode	Nosync	DMode	TY1	TY0	ID1	ID0	AM	0	0	0
	(6230h)			0	1	1	0	0	0	1	0	0	0	1	1	0	0	0	0
R12h	Sleep mode	0	1	0	0	DSLP	0	1	1	0	1	1	0	0	1	1	0	0	1
	(0D99h)			0	0	0	0	1	1	0	1	1	0	0	1	1	0	0	1
R15h	Entry mode	0	1	1	0	1	1	0	0	0	0	0	0	0	1	INVDOT	INVDEN	INVHS	INVVS
	(B010h)			1	0	1	1	0	0	0	0	0	0	0	1	0	0	0	0
R16h	Horizontal Porch	0	1	0	0	0	0	0	0	0	0	HBP7	HBP6	HBP5	HBP4	HBP3	HBP2	HBP1	HBP0
	(001Dh)			0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1
R17h	Vertical Porch	0	1	VFP7	VFP6	VFP5	VFP4	VFP3	VFP2	VFP1	VFP0	VBP7	VBP6	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0
	(0003h)			0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	1

(continued)

Reg#	Register	R/W	D/C	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R1Eh	Power control (5)	0	1	0	0	0	0	0	0	0	0	nOTP	0	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0
R20h	Uniformity	0	1	1	0	1	1	0	0	0	0	1	1	ENSVIN	0	1	0	1	1
	(B0EBh)			1	0	1	1	0	0	0	0	1	1	1	0	1	0	1	1
R22h	RAM data write	0	1	Data[17:0] mapping depends on the interface setting															
	RAM data read	1	1																
R25h	Frame Frequency	0	1	OSC3	OSC2	OSC1	OSC0	0	0	0	0	0	0	0	0	0	0	0	0
	(8000h)			1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R26h	Analogue Setting	0	1	0	RW_T	VCB	RLTM	ENN	0	0	0	0	0	0	0	0	0	0	0
	(3800h)			0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0
R28h	VCOM OTP (000Ah)	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0
R29h	VCOM OTP (80C0h)	0	1	1	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0
R30h	γ control (1)	0	1	0	0	0	0	0	PKP12	PKP11	PKP10	0	0	0	0	0	PKP02	PKP01	PKP00
R31h	γ control (2)	0	1	0	0	0	0	0	PKP32	PKP31	PKP30	0	0	0	0	0	PKP22	PKP21	PKP20
R32h	γ control (3)	0	1	0	0	0	0	0	PKP52	PKP51	PKP50	0	0	0	0	0	PKP42	PKP41	PKP40
R33h	γ control (4)	0	1	0	0	0	0	0	PRP12	PRP11	PRP10	0	0	0	0	0	PRP02	PRP01	PRP00
R34h	γ control (5)	0	1	0	0	0	0	0	PKN12	PKN11	PKN10	0	0	0	0	0	PKN02	PKN01	PKN00
R35h	γ control (6)	0	1	0	0	0	0	0	PKN32	PKN31	PKN30	0	0	0	0	0	PKN22	PKN21	PKN20
R36h	γ control (7)	0	1	0	0	0	0	0	PKN52	PKN51	PKN50	0	0	0	0	0	PKN42	PKN41	PKN40
R37h	γ control (8)	0	1	0	0	0	0	0	PRN12	PRN11	PRN10	0	0	0	0	0	PRN02	PRN01	PRN00
R3Ah	γ control (9)	0	1	0	0	0	VRP14	VRP13	VRP12	VRP11	VRP10	0	0	0	0	VRP03	VRP02	VRP01	VRP00
R3Bh	γ control (10)	0	1	0	0	0	VRN14	VRN13	VRN12	VRN11	VRN10	0	0	0	0	VRN03	VRN02	VRN01	VRN00
R41h	Vertical scroll control (1)	0	1	0	0	0	0	0	0	0	VL18	VL17	VL16	VL15	VL14	VL13	VL12	VL11	VL10
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R42h	Vertical scroll control (2)	0	1	0	0	0	0	0	0	0	VL28	VL27	VL26	VL25	VL24	VL23	VL22	VL21	VL20
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R44h	Vertical RAM address position	0	1	VEA7	VEA6	VEA5	VEA4	VEA3	VEA2	VEA1	VEA0	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0
	(EF00h)			1	1	1	0	1	1	1	1	0	0	0	0	0	0	0	0
R45h	Horizontal RAM address start position	0	1	0	0	0	0	0	0	0	HSA8	HSA7	HSA6	HSA5	HSA4	HSA3	HSA2	HSA1	HSA0
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R46h	Horizontal RAM address end position	0	1	0	0	0	0	0	0	0	HEA8	HEA7	HEA6	HEA5	HEA4	HEA3	HEA2	HEA1	HEA0
	(013Fh)			0	0	0	0	0	0	0	1	0	0	1	1	1	1	1	1
R48h	First window start	0	1	0	0	0	0	0	0	0	SS18	SS17	SS16	SS15	SS14	SS13	SS12	SS11	SS10
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R49h	First window end	0	1	0	0	0	0	0	0	0	SE18	SE17	SE16	SE15	SE14	SE13	SE12	SE11	SE10
	(00EFh)			0	0	0	0	0	0	0	0	1	1	1	0	1	1	1	1
R4Ah	Second window start	0	1	0	0	0	0	0	0	0	SS28	SS27	SS26	SS25	SS24	SS23	SS22	SS21	SS20
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R4Bh	Second window end	0	1	0	0	0	0	0	0	0	SE28	SE27	SE26	SE25	SE24	SE23	SE22	SE21	SE20
	(00EFh)			0	0	0	0	0	0	0	0	1	1	1	0	1	1	1	1
R4Eh	Set GDDRAM X address counter	0	1	0	0	0	0	0	0	0	XAD8	XAD7	XAD6	XAD5	XAD4	XAD3	XAD2	XAD1	XAD0
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R4Fh	Set GDDRAM Y address counter	0	1	0	0	0	0	0	0	0	0	YAD7	YAD6	YAD5	YAD4	YAD3	YAD2	YAD1	YAD0
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Note: In R01h, bits REV, BGR, RL, CM will override the corresponding hardware pins settings.
Setting R28h as 0x0006 is required before setting R25h and R29h registers.

9 COMMAND DESCRIPTION (TBC)

Index (IR)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	0	0	0	0	0	0	0	0	0	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

The index instruction specifies the RAM control indexes (R00h to RFFh). It sets the register number in the range of 00000000 to 11111111 in binary form. But do not access to Index register and instruction bits which do not have it's own index register.

Device Code Read (R00h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R	1	1	0	0	1	1	0	0	1	0	0	0	1	1	0	0	1

If this register is read forcibly, 9919h is read in 16 bit mode and 99h is read continuously in 8 bit mode.

Oscillator (R00h) (POR = 0000h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	OSCEN
POR		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

OSCEN: The oscillator will be turned on when OSCEN = 1, off when OSCEN = 0.

Driver Output Control (R01h) (POR = 3AEFh)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	RL	REV	GD	BGR	SM	TB	0	MUX7	MUX6	MUX5	MUX4	MUX3	MUX2	MUX1	MUX0
POR		0	0	1	1	1	0	1	0	1	1	1	0	1	1	1	1

REV: Displays all character and graphics display sections with reversal when REV = "1". Since the grayscale level can be reversed, display of the same data is enabled on normally white and normally black panels. Source output level is indicated below.

REV	RGB data	Source Output level	
		Vcom = "L"	Vcom = "H"
0	00000H : 3FFFFH	V63 : V0	V0 : V63
1	00000H : 3FFFFH	V0 : V63	V63 : V0

GD: Selects the 1st output Gate

GD		Left Side	Right Side
0	Normal	G1, 3, 5,…, 239	G240, 218, … , 4, 2
1	Flip	G2, 4, 6,…, 240	G239, 317, … , 3, 1

BGR: Selects the order from RGB to BGR in writing 18-bit pixel data in the GDDRAM.
When BGR = "0" <R><G><B> color is assigned from S1.
When BGR = "1" <B><G><R> color is assigned from S1.

SM: Change scanning order of gate driver.

SM	Gate scan squence (GD='0')
0	G1, G2, G3……G240 (left and right gate interlaced)
1	G1, G3, ……G239, G2, G4, ……G240

See "Scan mode setting" on next page.

RL: Selects the output shift direction of the source driver.

When RL = "1", S1 shifts to S960 and <R><G><B> color is assigned from S1.

When RL = "0", S960 shifts to S1 and <R><G><B> color is assigned from S960.

Set RL bit and BGR bit when changing the dot order of R, G and B. RL setting will be ignored when display with RAM (Dmode[1:0] = 00).

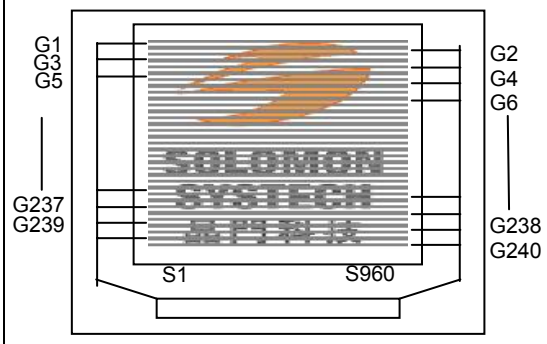
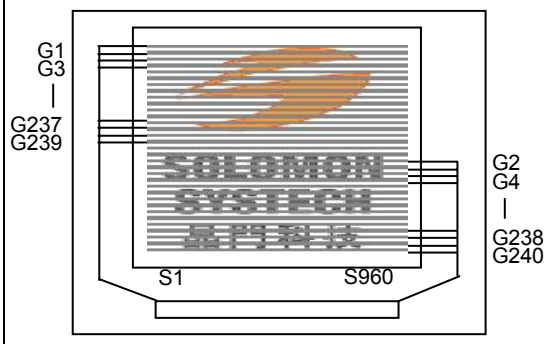
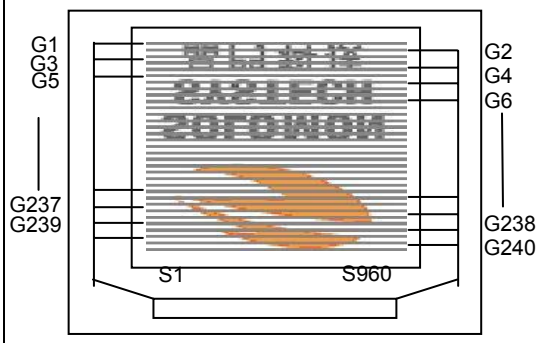
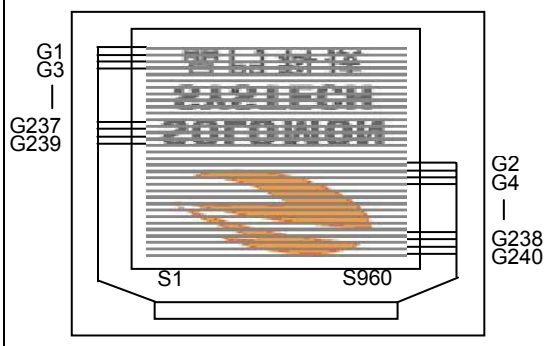
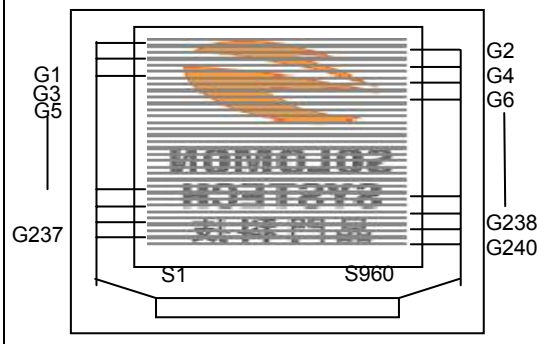
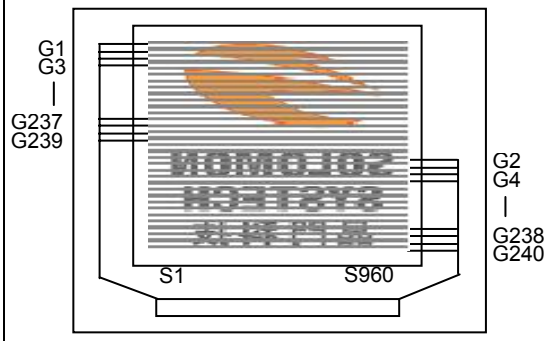
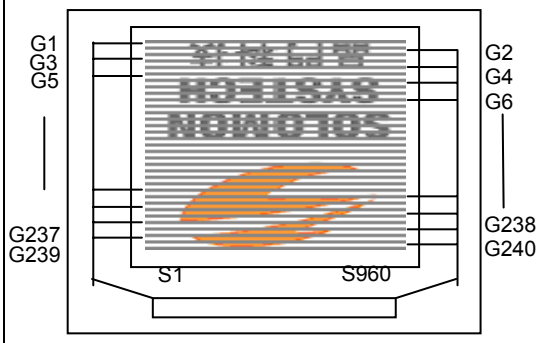
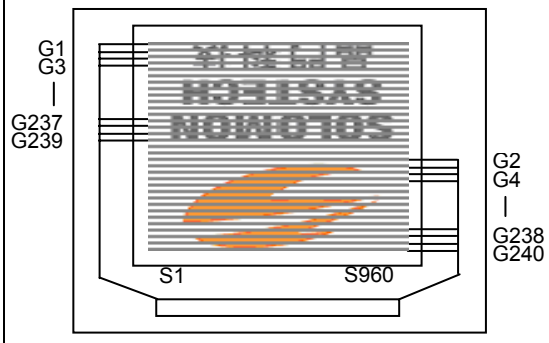
MUX[7:0]: Specify number of lines for the LCD driver. MUX[7:0] settings cannot exceed 240.
Remark: When using the partial display, the output for non-display area will be minimum voltage.

TB

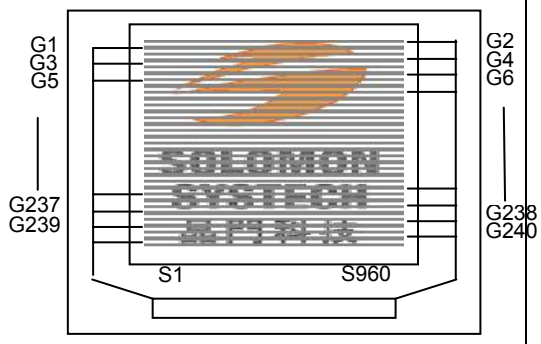
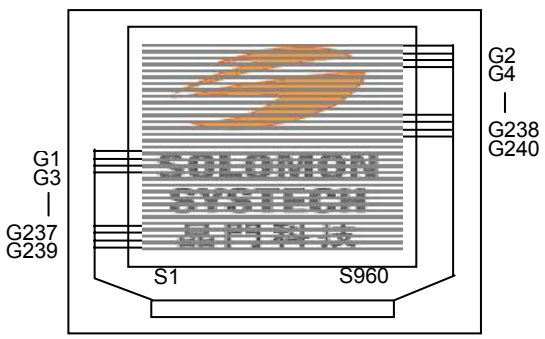
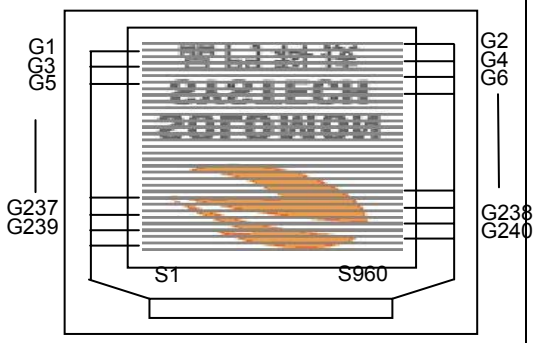
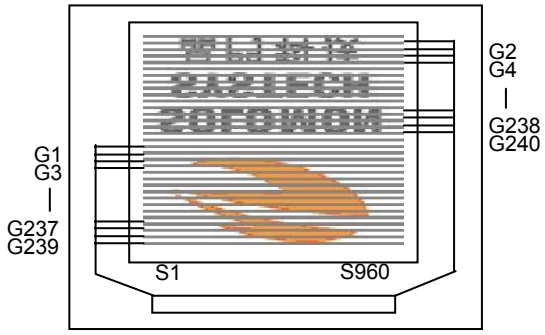
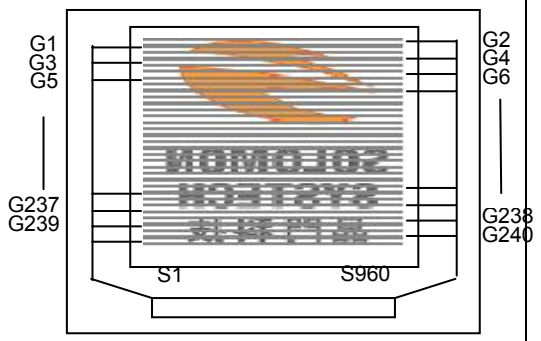
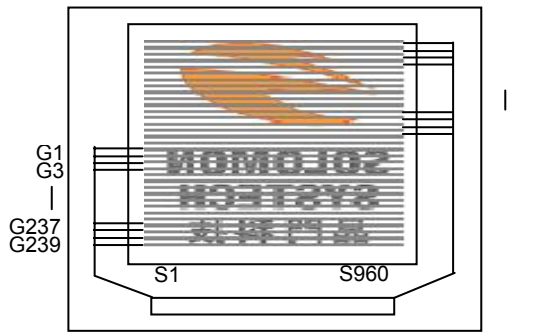
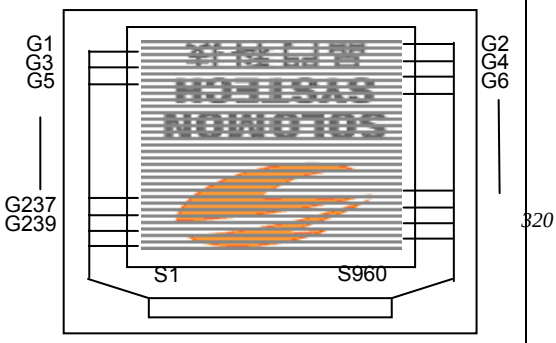
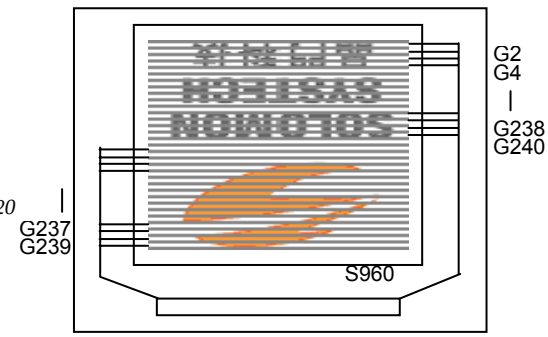
When TB = 1, scan from G1 to G240

When TB = 0, scan from G240 to G1

GD=’0’, G1 is the 1st gate output channel, gate output sequence is G1, G2, G3, …, G239, G240.

	SM = 0	SM = 1
TB = 1 RL = 1		
TB = 0 RL = 1		
TB = 1 RL = 0		
TB = 0 RL = 0		

GD=’1’, G1 is the 1st gate output channel, gate output sequence is G2, G1, G4, G3, …, G240, G239.

	SM = 0	SM = 1
TB = 1 **RL = 1**		
TB = 0 **RL = 1**		
TB = 1 **RL = 0**		
TB = 0 **RL = 0**		

LCD-Driving-Waveform Control (R02h) (POR = 0000h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	FLD	ENWS	B/C	EOR	WSMD	NW7	NW6	NW5	NW4	NW3	NW2	NW1	NW0
POR		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

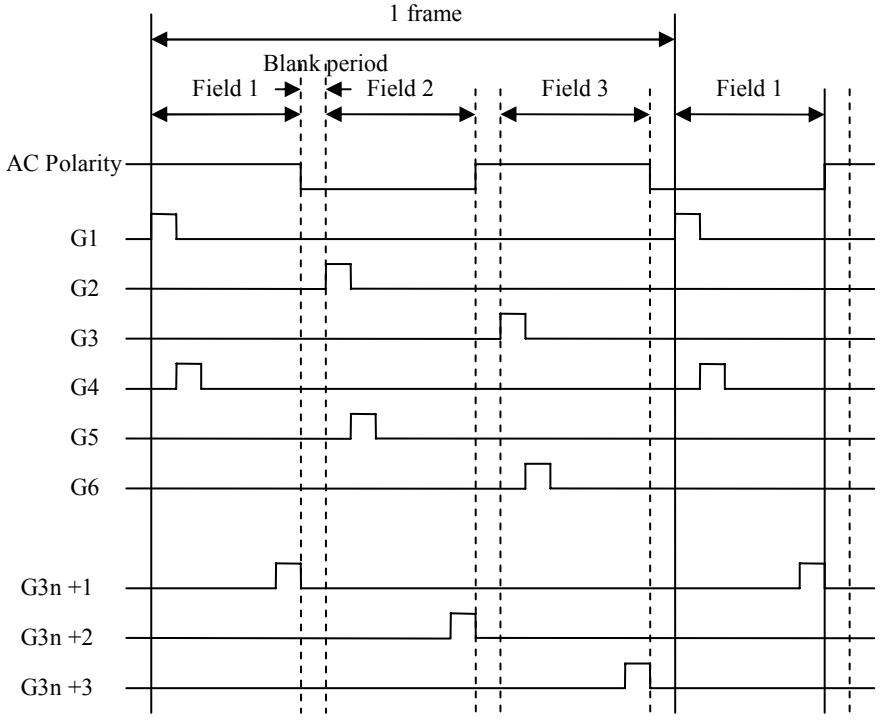
FLD: Set display in interlace drive mode to protect from flicker. It splits one frame into 3 fields and drive.
When FLD = 1, it is 3 field driving, which also limit VBP = 1.
When FLD = 0, it is normal driving.

The following figure shows the gate selection when the 3-field invension is enabled and the output waveform of the 3-field interlaced driving.

Table 9-1: 3-field interlace driving

TB = 1			TB = 0		
Gate	FLD = 0	FLD = 1	Gate	FLD = 0	FLD = 1
G1	X		G240	X	
G2	X		G239	X	
G3	X	X	G238	X	X
G4	X		G237	X	
G5	X		G236	X	
	X	X		X	X
	X			X	
	X			x	
G238	X		G3	X	
G239	X		G2	X	
G240	X	X	G1	X	X

Figure 9-1: gate output timing in 3-field interlacing driving



B/C: Select the liquid crystal drive waveform VCOM.

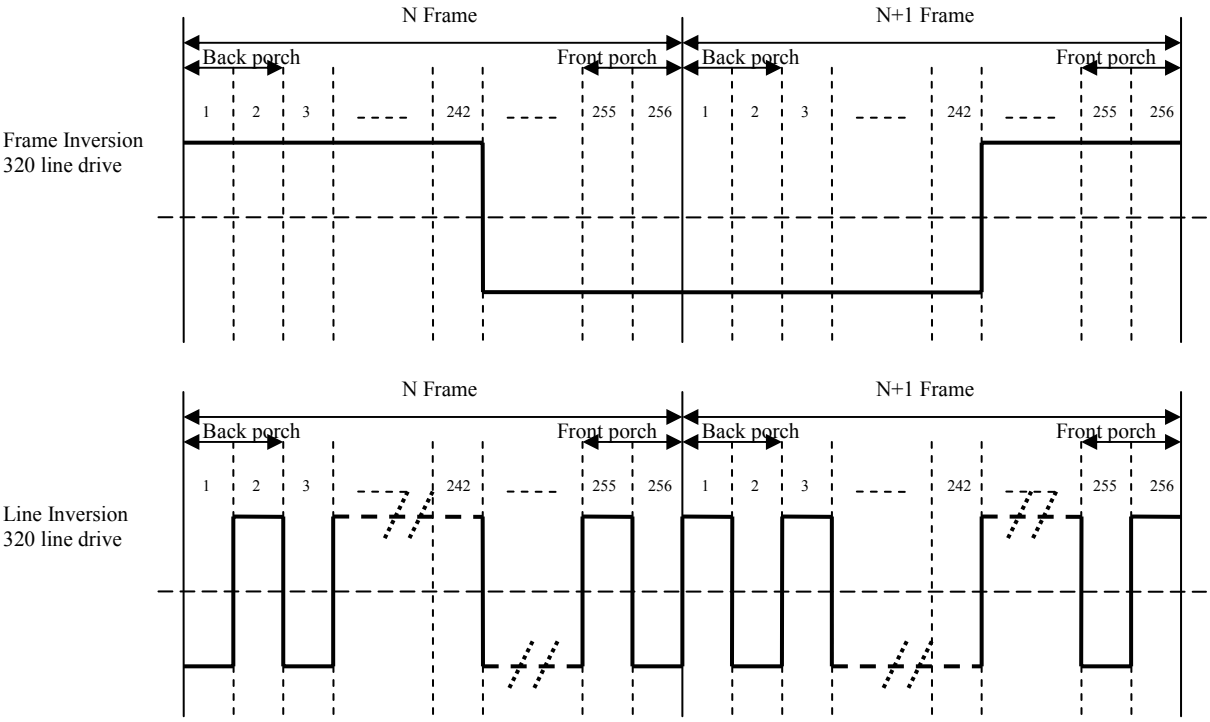
When B/C = 0, frame inversion of the LCD driving signal is enabled.

When B/C = 1, a N-line inversion waveform is generated and alternates in a N-line equals to NW[7:0]+1.

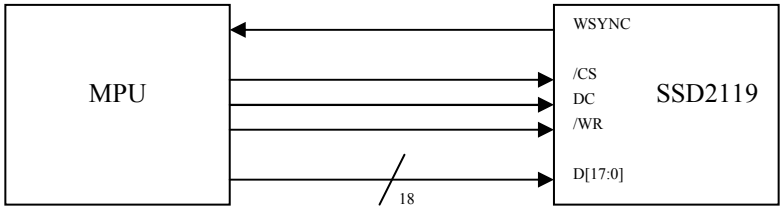
EOR: When B/C = 1 and EOR = 1, the odd/even frame-select signals and the N-line inversion signals are EORed for alternating drive. EOR is used when the LCD is not alternated by combining the set values of the lines of the LCD driven and the N-lines.

NW[7:0]: Specify the number of lines that will alternate at the N-line inversion setting (B/C = 1). N-line is equal to NW[7:0]+1.

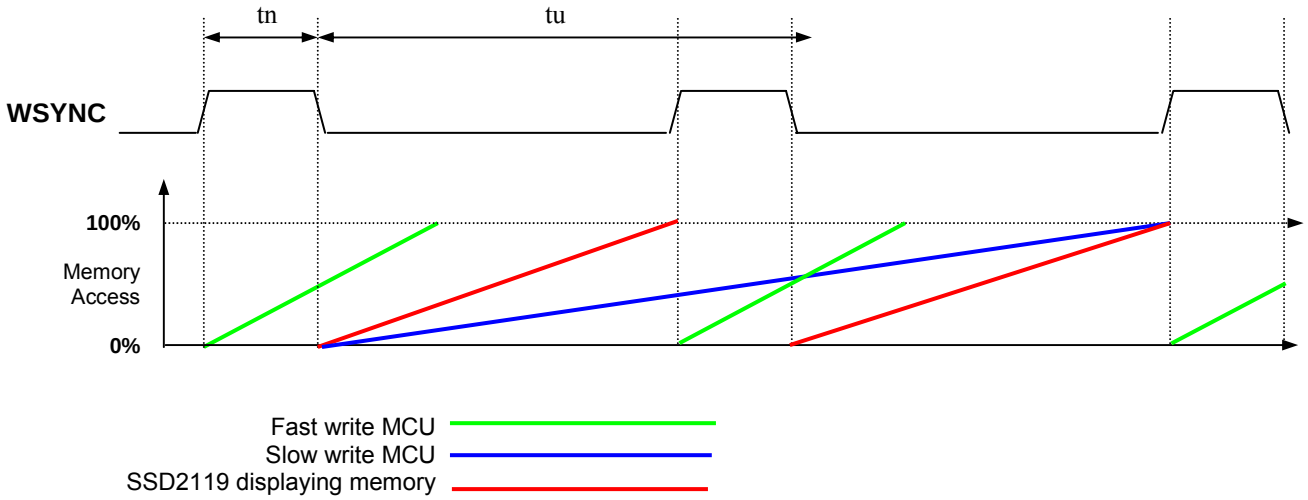
Figure 9-2: Line Inversion AC Driver



ENWS: When ENWS = 1, it enables WSYNC output pin. Mode1 or Mode2 is selected by WSMD. When ENWS = 0(POR), it disables WSYNC feature, the WSYNC output pin will be high-impedance.

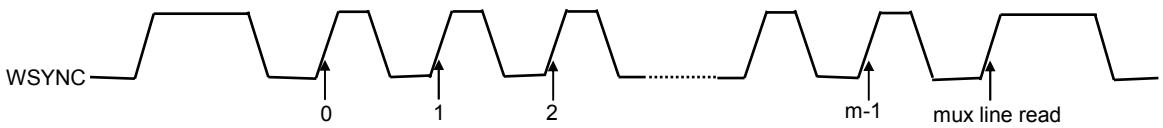


WSMD = 0 is **mode1**, the waveform of WSYNC output will be:



tn is the time when there is No Update of LCD screen from on-chip ram content.
tu is the time when the LCD screen is updating based on on-chip ram content.
e.g. fosc = 380KHz, for 320mux, tn = 282us (6 lines), tu =15.06ms (320 lines)

WSMD = 1 is **mode2**, the waveform of WSYNC output will be:



For fast write MCU: MCU should start to write new frame of ram data just after rising edge of long WSYNC pulse and should be finished well before the rising edge of the next long WSYNC pulse.
e.g. 5MHz 8 bit parallel write cycle for 18 bit color depth, or 3MHz 8 bit parallel write cycle for 16 bit color depth.

For slow write MCU (Half the write speed of fast write): MCU should start to write new frame ram data after the rising edge of the first short WSYNC pulse and must be finished within 2 frames time.
e.g. 2.5MHz 8 bit parallel write cycle for 18 bit color depth.
* Usually, **mode2** is for slower MCU, while **mode1** is for fast MCU.

Power control 1 (R03h) (POR = 6A64h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	DCT3	DCT2	DCT1	DCT0	BT2	BT1	BT0	0	DC3	DC2	DC1	DC0	AP2	AP1	AP0	0
POR		0	1	1	0	1	0	1	0	0	1	1	0	0	1	0	0

DCT[3:0]: Set the step-up cycle of the step-up circuit for 8-color mode (CM = V_{DDIO}). When the cycle is accelerated, the driving ability of the step-up circuit increases, but its current consumption increases too. Adjust the cycle taking into account the display quality and power consumption.

DCT3	DCT2	DCT1	DCT0	Step-up cycle
0	0	0	0	Fline × 24
0	0	0	1	Fline × 16
0	0	1	0	Fline × 12
0	0	1	1	Fline × 8
0	1	0	0	Fline × 6
0	1	0	1	Fline × 5
0	1	1	0	Fline × 4
0	1	1	1	Fline × 3
1	0	0	0	Fline × 2
1	0	0	1	Fline × 1
1	0	1	0	fosc / 4
1	0	1	1	fosc / 6
1	1	0	0	fosc / 8
1	1	0	1	fosc / 10
1	1	1	0	fosc / 12
1	1	1	1	fosc / 16

* Fline = Line frequency
fosc = Internal oscillator frequency (~380KHz)

BT[2:0]: Control the step-up factor of the step-up circuit. Adjust the step-up factor according to the power-supply voltage to be used.

BT2	BT1	BT0	V_{GH} output	V_{GL} output	V_{GH} booster ratio	V_{GL} booster ratio
0	0	0	3 x V_{CIX2}	-(V_{GH}) + V_{CI}	+6	-5
0	0	1	3 x V_{CIX2}	-(V_{GH}) + V_{CIX2}	+6	-4
0	1	0	3 x V_{CIX2}	-(V_{CIX2})	+6	-2
0	1	1	2 x V_{CIX2} + V_{CI}	-(V_{GH})	+5	-5
1	0	0	2 x V_{CIX2} + V_{CI}	-(V_{GH}) + V_{CI}	+5	-4
1	0	1	2 x V_{CIX2} + V_{CI}	-(V_{GH}) + V_{Cix2}	+5	-3
1	1	0	2 x V_{CIX2}	-(V_{GH})	+4	-4
1	1	1	2 x V_{CIX2}	-(V_{GH}) + V_{CI}	+4	-3

DC[3:0]: Set the step-up cycle of the step-up circuit for 262k-color mode (CM = V_{SS}). When the cycle is accelerated, the driving ability of the step-up circuit increases, but its current consumption increases too. Adjust the cycle taking into account the display quality and power consumption.

DC3	DC2	DC1	DC0	Step-up cycle
0	0	0	0	Fline × 24
0	0	0	1	Fline × 16
0	0	1	0	Fline × 12
0	0	1	1	Fline × 8
0	1	0	0	Fline × 6
0	1	0	1	Fline × 5
0	1	1	0	Fline × 4
0	1	1	1	Fline × 3
1	0	0	0	Fline × 2
1	0	0	1	Fline × 1
1	0	1	0	fosc / 4
1	0	1	1	fosc / 6
1	1	0	0	fosc / 8
1	1	0	1	fosc / 10
1	1	1	0	fosc / 12
1	1	1	1	fosc / 16

* Fline = Line frequency
fosc = Internal oscillator frequency (~380KHz)

AP[2:0]: Adjust the amount of current from the stable-current source in the internal operational amplifier circuit. When the amount of current becomes large, the driving ability of the operational-amplifier circuits increase. Adjust the current taking into account the power consumption. During times when there is no display, such as when the system is in a sleep mode.

AP2	AP1	AP0	Op-amp power
0	0	0	Least
0	0	1	Small
0	1	0	Small to medium
0	1	1	Medium
1	0	0	Medium to large
1	0	1	Large
1	1	0	Large to Maximum
1	1	1	Maximum

Display Control (R07h) (POR = 0000h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	PT1	PT0	VLE2	VLE1	SPT	0	0	GON	DTE	CM	0	D1	D0
POR		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PT[1:0]: Normalize the source outputs when non-displayed area of the partial display is driven.

VLE[2:1]: When VLE1 = 1 or VLE2 = 1, a vertical scroll is performed in the 1st screen by taking data VL17-0 in R41h register. When VLE1 = 1 and VLE2 = 1, a vertical scroll is performed in the 1st and 2nd screen by VL1[8:0] and VL2[8:0] respectively.

SPT: When SPT = "1", the 2-division LCD drive is performed.

CM: 8-color mode setting.
When CM = 1, 8-color mode is selected.
When CM = 0, 8-color mode is disable.

GON: Gate off level becomes VGH when GON = "0".

DTE: When GON = "1" and DTE = "0", all gate outputs become VGL. When GON = "1" and DTE = "1", selected gate wire becomes VGH, and non-selected gate wires become VGL.

D[1:0]: Display is on when D1 = "1" and off when D1 = "0". When off, the display data remains in the GDDRAM, and can be displayed instantly by setting D1 = "1". When D1= "0", the display is off with all of the source outputs set to the GND level. Because of this, the driver can control the charging current for the LCD with AC driving. When D[1:0] = "01", the internal display is performed although the display is off. When D[1:0] = "00", the internal display operation halts and the display is off. Control the display on/off while control GON and DTE.

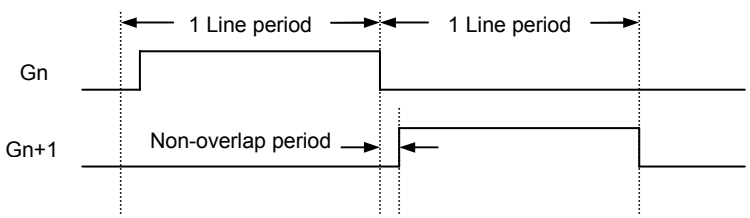
GON	DTE	D1	D0	Internal Display Operation	Source output	Gate output
0	0	0	0	Halt	GND	V_{GH}
0	0	0	1	Operation	GND	V_{GH}
1	0	0	1	Operation	GND	V_{GOFFL}
1	0	1	1	Operation	Grayscale level output	V_{GOFFL}
1	1	1	1	Operation	Grayscale level output	Selected gate line: V_{GH} Non-selected gate line: V_{GOFFL}

Frame Cycle Control (R0Bh) (POR = 5308h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	NO1	NO0	SDT1	SDT0	0	EQ2	EQ1	EQ0	DIV1	DIV0	SDIV	SRTN	RTN3	RTN2	RTN1	RTN0
POR		0	1	0	1	0	0	1	1	0	0	0	0	1	0	0	0

NO[1:0]: Sets amount of non-overlap of the gate output.

NO1	NO0	Amount of non-overlap
0	0	reserved
0	1	1 clock cycle (POR)
1	0	2 clock cycle
1	1	3 clock cycle

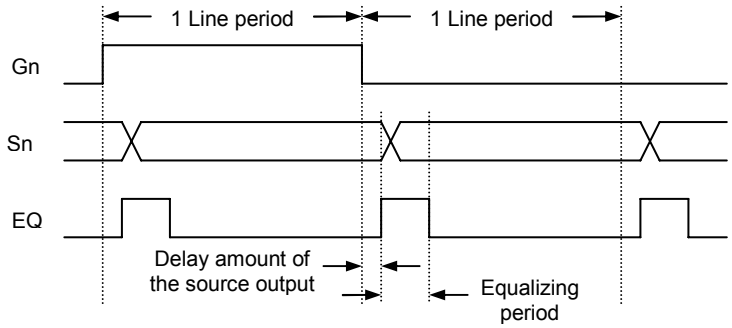


SDT[1:0]: Set delay amount from the gate output signal falling edge of the source outputs.

SDT1	SDT0	Delay amount of the source output
0	0	0 clock cycle
0	1	1 clock cycle (POR)
1	0	2 clock cycle
1	1	3 clock cycle

EQ[2:0]: Sets the equalizing period.

EQ2	EQ1	EQ0	EQ period
0	0	0	No EQ
0	0	1	2 clock cycle
0	1	0	3 clock cycle
0	1	1	4 clock cycle
1	0	0	5 clock cycle
1	0	1	6 clock cycle
1	1	0	7 clock cycle
1	1	1	8 clock cycle



DIV[1:0]: Set the division ratio of clocks for internal operation. Internal operations are driven by clocks which frequency is divided according to the DIV1-0 setting.

DIV1	DIV0	Division Ratio
0	0	1
0	1	2
1	0	4
1	1	8

* fosc = internal oscillator frequency, ~380kHz

SDIV: When SDIV = 1, DIV1-0 value will be count. When SDIV = 0, DIV1-0 value will be auto determined.

SRTN: When SRTN =1, RTN3-0 value will be count. When SRTN = 0, RTN3-0 value will be auto determined.

RTN[3:0]: Set the no. of clocks in each line. The total number will be the decimal value of RTN3-0 plus 16. e.g. if RTN3-0 = "1010h", the total number of clocks in each line = 10 +16 = 26 clocks.

Frame frequency calculation

For DMode = '0'

$$Frame\_frequency = \frac{Fosc}{div \times (rtn + 16) \times (mux + vbp + vfp + 3)}$$

where *Fosc* = internal oscillator frequency
div = Division ratio determined by DIV[1:0]
rtn = RTN[3:0]
mux = MUX[8:0]
vbp = VBP[7:0]
vfp = VFT[7:0]

for default values of SSD2119
Fosc = ~380KHz, DIV[1:0] = '00', RTN[3:0] = 8, MUX[8:0] = 239, VBP[7:0] = 3, VFP[7:0] = 1,

Frame frequency = $\frac{380K}{1 \times (8+16) \times (239+3+1+3)} = \frac{380K}{1 \times 24 \times 246} = 65Hz$

Power Control 2 (R0Ch) (POR = 0004h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	VRC2	VRC1	VRC0
POR		0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

VRC[2:0]: Adjust VCIX2 output voltage. The adjusted level is indicated in the chart below VRC2-0 setting.

VRC2	VRC1	VRC0	VCIX2 voltage
0	0	0	5.1V
0	0	1	5.3V
0	1	0	5.5V
0	1	1	5.7V
1	0	0	5.9V
1	0	1	6.1V
1	1	0	Reserved
1	1	1	Reserved

Note: The above setting is valid when VCI has high enough voltage supply for boosting up the required voltage.
The above setting is assumed 100% booster efficiency. Please refer to DC Characteristics for detail.
Data from the above table are based on targeted VCIX2 output, actual VCIX2 voltage depends on VCI, booster efficiency and panel loading.
Data from the above table are measured at VCI=3.3V and without panel loading.

Power Control 3 (R0Dh) (POR = 0009h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	VRH3	VRH2	VRH1	VRH0
POR*		0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1

VRH[3:0]: Set amplitude magnification of V_{LCD63}. These bits amplify the V_{LCD63} voltage 1.78 to 3.00. times the Vref voltage set by VRH[3:0].

VRH3	VRH2	VRH1	VRH0	V_{LCD63} Voltage
0	0	0	0	Vref x 2.810
0	0	0	1	Vref x 2.900
0	0	1	0	Vref x 3.000
0	0	1	1	Vref x 1.780
0	1	0	0	Vref x 1.850
0	1	0	1	Vref x 1.930
0	1	1	0	Vref x 2.020
0	1	1	1	Vref x 2.090
1	0	0	0	Vref x 2.165
1	0	0	1	Vref x 2.245
1	0	1	0	Vref x 2.335
1	0	1	1	Vref x 2.400
1	1	0	0	Vref x 2.500
1	1	0	1	Vref x 2.570
1	1	1	0	Vref x 2.645
1	1	1	1	Vref x 2.725

*****Vref is the internal reference voltage equals to 2.0V.

Power Control 4 (R0Eh) (POR = 3200h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	VCOMG	VDV4	VDV3	VDV2	VDV1	VDV0	0	0	0	0	0	0	0	0
POR*		0	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0

VcomG: When VcomG = "1", it is possible to set output voltage of VcomL to any level, and the instruction (VDV4-0) becomes available. When VcomG = "0", VcomL output is fixed to Hi-z level, VCIM output for VcomL power supply stops, and the instruction (VDV4-0) becomes unavailable. Set VcomG according to the sequence of power supply setting flow as it relates with power supply operating sequence.

VDV[4:0]: Set the alternating amplitudes of Vcom at the Vcom alternating drive. These bits amplify 0.6 to 1.23 times the VLCD63 voltage. When VcomG = "0", the settings become invalid. External voltage at VcomR is referenced when VDV = "01111".

VCOML = 0.9475*VCOMH - VCOMA

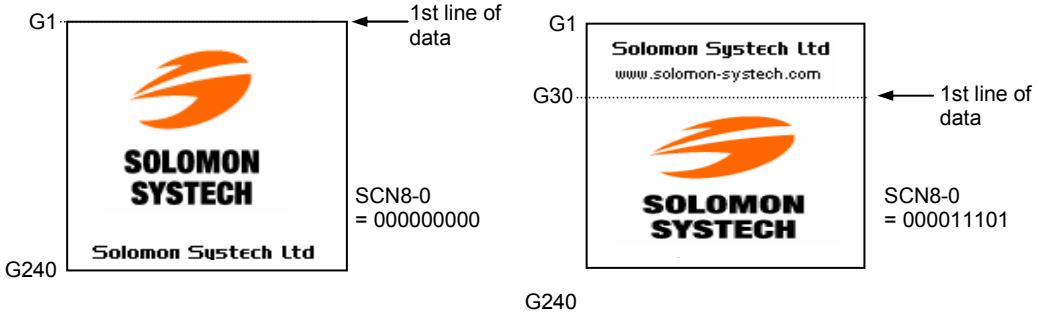
VDV4	VDV3	VDV2	VDV1	VDV0	Vcom Amplitude
0	0	0	0	0	VLCD63 x 0.60
0	0	0	0	1	VLCD63 x 0.63
0	0	0	1	0	VLCD63 x 0.66
		:			: Step = 0.03 :
0	1	1	0	1	VLCD63 x 0.99
0	1	1	1	0	VLCD63 x 1.02
0	1	1	1	1	Reference from external variable resistor
1	0	0	0	0	VLCD63 x 1.05
1	0	0	0	1	VLCD63 x 1.08
		:			: Step = 0.03 :
1	0	1	0	1	VLCD63 x 1.20
1	0	1	1	0	VLCD63 x 1.23
1	0	1	1	1	Reserved
1	1	*	*	*	Reserved

Note: Vcom amplitude < 6V

Gate Scan Position (R0Fh) (POR = 0000h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	SCN8	SCN7	SCN6	SCN5	SCN4	SCN3	SCN2	SCN1	SCN0
POR		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SCN[8:0]: Set the scanning starting position of the gate driver. The valid range is from 1 to 240.



Sleep mode (R10h, R12h)

Reg#	R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R10h	W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SLP
	POR		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R12h	W	1	0	0	DSLP	0	VSH2	VSH1	VSH0	1	1	0	0	1	1	0	0	1
	POR		0	0	0	0	1	1	0	1	1	0	0	1	1	0	0	1

SLP:
When SLP = 1, the driver enters normal sleep mode if DSLP = 0. The driver will enter deep sleep mode if DSLP=1.

When SLP = 0, the driver leaves the sleep mode.

In normal sleep mode, the internal display operations and step-up circuits are halted. GDDRAM data and instruction setting are retained when exit sleep mode.

In deep sleep mode DSLP=1, internal logic power is turned off to further reduce power consumption. GDDRAM data needed to be sent again after exit deep sleep mode.

For example :

Normal sleep mode command
R10, x0001 (enter sleep mode)
R07, x0000 (display off)

Deep sleep mode command
R28, x0006 (enable test command)
R10, x0001 (enter sleep mode)
R12, x2999 (enable deep sleep function)
R07, x0000 (display off)

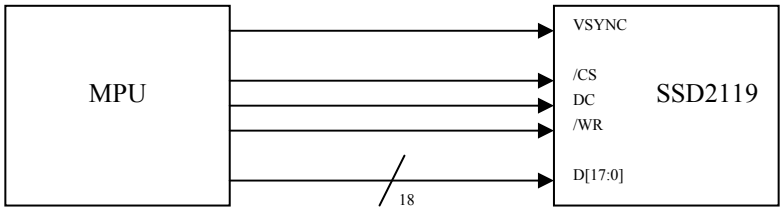
VSH[2:0]: Vcore voltage select

VSH[2:0]	Vcore
000	1.3V
001	1.4V
010	1.5V
011	1.6V
100	1.7V
101	1.8V
110	1.9V (por)
111	2.0V

Entry Mode (R11h) (POR = 6230h)

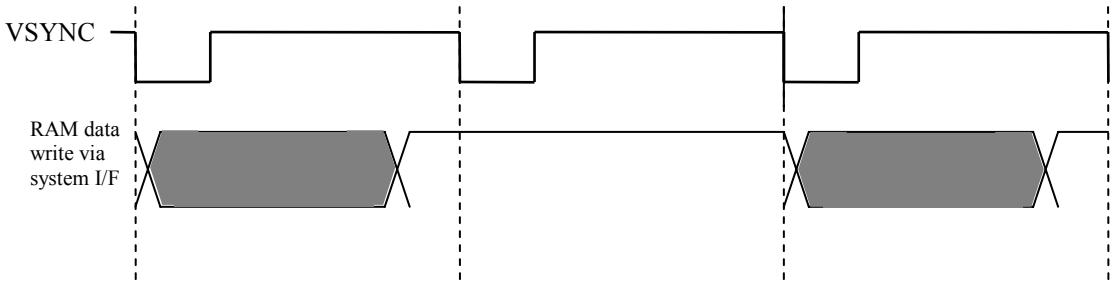
R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	VSMode	DFM1	DFM0	0	DenMode	Wmode	Nosync	Dmode	TY1	TY0	ID1	ID0	AM	0	0	0
POR		0	1	1	0	0	0	1	0	0	0	1	1	0	0	0	0

VSMode: When VSMode = 1 at DMode = "0", the frame frequency will be dependent on VSYNC.



In VSYNC interface operation, the internal display operation is synchronized with the VSYNC signal. By writing data to the internal RAM at faster than the calculated minimum speed (internal display oerpation speed + buffer), it becomes possible to rewrite the moving picture data without flickering the display and display a moving picture via system interface.

The display operation is performed in synchronization with the internal clock signal generated from the internal oscillator and the VSYNC signal. The display data is written in the internal RAM so that the SSD2119 rewrites the data only within the moving picture area and minimize the number of data transfer required for moving picture display. Therefore, the SSD2119 can write data via VSYNC interface in high speed with low power consumption.



The VSYNC interface has the minimum for RAM data write speed and internal clock frequency, which must be more than the values calculated from the following formulas, respectively.

$$Fosc[Hz] = Frame\_frequency * (mux + vfp + vbp + 3) * (rtn + 16) * (div)$$

$$RAMWriteSpeed(\min)[Hz] > \frac{320 * mux}{(vbp + mux - m\arg ins) * (rtn + 16) * \frac{1}{fosc}}$$

where *Fosc* = internal oscillator frequency
div = Division ratio determined by DIV[1:0]
rtn = RTN[3:0]
mux = MUX[8:0]
vbp = VBP[7:0]
vfp = VFT[7:0]

Note: When RAM write operation is not started right after the falling edge of VSYNC, the time from the falling edge of VSYNC until the start of RAM write operation must also be taken into account.

DFM[1:0]: Set the color display mode.

DFM1	DFM0	Color mode
1	1	65k color (POR)
1	0	262k color

DenMode:

DenMode=1 : RGB interface ignore HSYNC, VSYNC pin and HBP, VBP
DenMode=0 : RGB interface control by HSYNC, VSYNC pin and HBP, VBP

When DenMode=1, Generic mode will write each input rgb pixel into RAM buffer, the window of ram buffer to be written defined by command R44h (define Y of window)m R45h (define X start),R46 (define X end), whenever the input RGB dimension is larger than the defined ram window, it wont have any effect.

Note: For RGB mode
When DenMode=1, DEN signal is necessary
When DenMode=0, DEN pin must connect to VDDIO

WMode:

WMode=1 : Write RAM from Generic RGB data (POR, if PS:00xx)
WMode=0 : Write RAM from SPI interface

Nosync:

Nosync=1 : Dmode change immediately
Nosync=0 : Dmode change Sync with on chip frame start

Dmode:

Dmode=1 : Display engine will be clocked by DOTCLK pin and onchip oscillator will be off (POR, if PS:00xx)
Dmode=0 : Display engine will be clocked by on chip oscillator and ignore DOTCLK pin

TY[1:0]: In 262k color mode, 16 bit parallel interface, there are three types of methods in writing data into the ram, Type A, B and C are described as below.

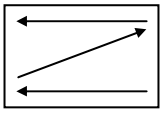
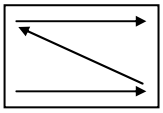
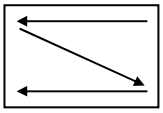
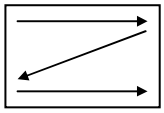
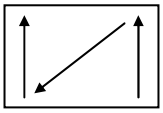
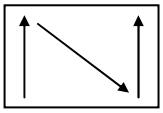
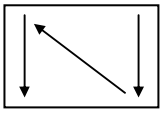
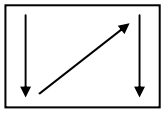
TY1	TY0	Writing mode
0	0	Type A
0	1	Type B
1	0	Type C

			Hardware pins																	
Interface	**Color mode**	**Cycle**	**D17**	**D16**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
16 bit	**262k Type A**	1st	R5	R4	R3	R2	R1	R0	x	x		G5	G4	G3	G2	G1	G0	x	x	
		2nd	B5	G4	B3	B2	B1	B0	x	x		R5	R4	R3	R2	R1	R0	x	x	
		3rd	G5	G4	G3	G2	G1	G0	x	x		B5	G4	B3	B2	B1	B0	x	x	
	262k Type B	1st	R5	R4	R3	R2	R1	R0	x	x		G5	G4	G3	G2	G1	G0	x	x	
		2nd	x	x	x	x	x	x	x	x		B5	G4	B3	B2	B1	B0	x	x	
	262k Type C	1st	R5	R4	R3	R2	R1	R0	x	x		G5	G4	G3	G2	G1	G0	x	x	
		2nd	B5	G4	B3	B2	B1	B0	x	x		x	x	x	x	x	x	x	x	

Remark : x Don't care bits
Not connected pins

ID[1:0]: The address counter is automatically incremented by 1, after data are written to the GDDRAM when ID[1:0] = "1". The address counter is automatically decremented by 1, after data are written to the GDDRAM when ID[1:0] = "0". The setting of incrementing or decrementing of the address counter can be made independently in each upper and lower bit of the address. The direction of the address when data are written to the GDDRAM is set with AM bits.

AM: Set the direction in which the address counter is updated automatically after data are written to the GDDRAM. When AM = "0", the address counter is updated in the horizontal direction. When AM = "1", the address counter is updated in the vertical direction. When window addresses are selected, data are written to the GDDRAM area specified by the window addresses in the manner specified with ID1-0 and AM bits.

	ID[1:0]="00" Horizontal: decrement Vertical: decrement	ID[1:0]="01" Horizontal: increment Vertical: decrement	ID[1:0]="10" Horizontal: decrement Vertical: increment	ID[1:0]="11" Horizontal: increment Vertical: increment
AM="0" Horizontal	00,00h  13F,EFh	00,00h  13F,EFh	00,00h  13F,EFh	00,00h  13F,EFh
AM="1" Vertical	00,00h  13F,EFh	00,00h  13F,EFh	00,00h  13F,EFh	00,00h  13F,EFh

Note: ID and AM functions are not supported in RGB mode

Generic Interface Control (R15h) (POR = B010h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	INVDOT	INVDEN	INVHS	INVVS
POR		1	0	1	1	0	0	0	0	0	0	0	1	0	0	0	0

INVDOT: sets the signal polarity of DOTCLK pin. When INVDOT = 0, data is latched at positive edge of DOTCLK. When INVDOT = 1, data is latched at negative edge of DOTCLK.

INVDEN: sets the signal polarity of DEN pin. When INVDEN = 0, DEN is active high. When INVDEN = 1, DEN is active low.

INVHS: sets the signal polarity of HSYNC pin. When INVHS = 0, HSYNC is active low. When INVHS = 1, HSYNC is active high.

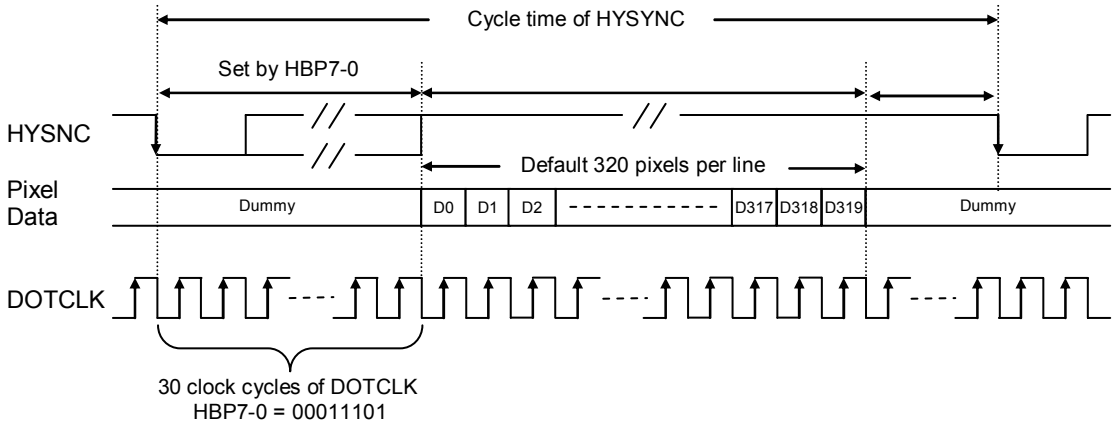
INVVS: sets the signal polarity of VSYNC pin. When INVVS = 0, VSYNC is active low. When INVVS = 1, VSYNC is active high.

Horizontal Porch (R16h) (POR = 001Dh)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	HBP7	HBP6	HBP5	HBP4	HBP3	HBP2	HBP1	HBP0
POR		0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1

HBP[7:0]: Set the delay period from falling edge of HSYNC signal to first valid data.

HBP7	HBP6	HBP5	HBP4	HBP3	HBP2	HBP1	HBP0	No. of clock cycle of DOTCLK
0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	1	2
				:				: Step = 1 :
0	0	0	1	1	0	1	0	27
0	0	0	1	1	0	1	1	28
0	0	0	1	1	1	0	0	29
0	0	0	1	1	1	0	1	30 (POR)
0	0	0	1	1	1	1	0	31
				:				: Step = 1 :
1	1	1	1	1	1	1	0	255
1	1	1	1	1	1	1	1	256



Vertical Porch (R17h) (POR = 0003h)

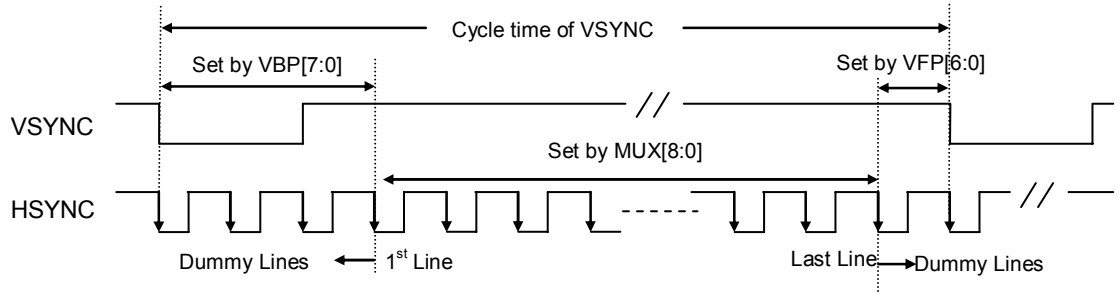
R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	VFP6	VFP5	VFP4	VFP3	VFP2	VFP1	VFP0	VBP7	VBP6	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0
POR		0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

VFP[6:0]: Set the delay period from the last valid line to the falling edge of VSYNC of the next frame. The line data within this delay period will be treated as dummy line.

VFP6	VFP5	VFP4	VFP3	VFP2	VFP1	VFP0	No. of clock cycle of HSYNC
0	0	0	0	0	0	0	1 (POR)
0	0	0	0	0	0	1	2
:	:						: Step = 1 :
1	1	1	1	1	1	0	127
1	1	1	1	1	1	1	128

VBP[7:0]: Set the delay period from falling edge of VSYNC to first valid line. The line data within this delay period will be treated as dummy line.

VBP7	VBP6	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0	No. of clock cycle of HSYNC
0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	1	2
0	0	0	0	0	0	1	0	3
0	0	0	0	0	0	1	1	4 (POR)
:								: Step = 1 :
1	1	1	1	1	1	1	0	255
1	1	1	1	1	1	1	1	256



Power Control 5 (R1Eh) (POR = 002Bh)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	nOTP	0	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0
POR*		0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	1

nOTP: nOTP equals to "0" after power on reset and VcomH voltage equals to programmed OTP value. When nOTP set to "1", setting of VCM[5:0] becomes valid and voltage of VcomH can be adjusted.

VCM[5:0]: Set the VcomH voltage if nOTP = "1". These bits amplify the VcomH voltage 0.36 to 0.99 times the VLCD63 voltage. Default value is "101001" when power on reset.

VCM5	VCM4	VCM3	VCM2	VCM1	VCM0	VcomH
0	0	0	0	0	0	VLCD63 x 0.36
0	0	0	0	0	1	VLCD63 x 0.37
			:			: Step = 0.01 :
1	1	1	1	1	0	VLCD63 x 0.98
1	1	1	1	1	1	VLCD63 x 0.99

Uniformity (R20h) (POR = B0EBh)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	1	0	1	1	0	0	0	0	1	1	ENSVIN	0	1	0	1	1
POR		1	0	1	1	0	0	0	0	1	1	1	0	1	0	1	1

ENSVIN: When ENSVIN = 1, uniformity improvement scheme is enabled
When ENSVIN = 0, uniformity improvement scheme is disabled

Write Data to GRAM (R22h)

R/W	DC	D[17:0]
W	1	WD[17:0] mapping depends on the interface setting

WD[17:0]: Transforms all the GDDRAM data into 18-bit, and writes the data. Format for transforming data into 18-bit depends on the interface used. SSD2119 selects the grayscale level according to the GDDRAM data. After writing data to GDDRAM, address is automatically updated according to AM bit and ID bit. Access to GDDRAM during stand-by mode is not available.

Read Data from GRAM (R22h)

R/W	DC	D[17:0]
R	1	RD[17:0] mapping depends on the interface setting

RD[17:0]: Read 18-bit data from the GDDRAM. When the data is read to the microcomputer, the first-word read immediately after the GDDRAM address setting is latched from the GDDRAM to the internal read-data latch. The data on the data bus (DB17–0) becomes invalid and the second-word read is normal. When bit processing, such as a logical operation, is performed, only one read can be processed since the latched data in the first word is used.

Frame Frequency Control (R25h) (POR = 8000h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	OSC3	OSC2	OSC1	OSC0	0	0	0	0	0	0	0	0	0	0	0	0
POR*		1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

OSC[3:0]: Set the frame frequency by OSC[3:0]

OSC[3:0]	Internal Oscillator Frequency (Hz)	Corresponding Frame Freq (Hz) (other registers are at POR value)
0000	295K	50
0010	325K	55
0101	354K	60

1000	380K	65
1010	413K	70
1100	443K	75
1110	472K	80

Analogue Setting (R26h) (POR = 7000h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	RW_T	VCB	RTLM	ENN	0	0	0	0	0	0	0	0	0	0	0
POR*		0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0

RW_T (RAM read/write timing)

RW_T=0 : ON Wordline after Bitlines Pre-charge OFF
RW_T=1 : ON Wordline before Bitlines Pre-charge OFF(por)

VCB (VCOM buffer)

VCB=1 : VCOML buffer off during VCOM output VCOMH (por)
VCB=0: VCOML buffer on even VCOM output VCOMH

RTLM (RAM read/write monitoring)

RTLM=1: RAM read/write monitoring ON (por)
RTLM=0: RAM read/write monitoring OFF

ENN (enable deep sleep mode of ram)

ENN=1 : stop precharge bitlines in sleep mode
ENN=0 : always precharge bitlines (por)

Suggested Code for R26H is x3800.

Vcom OTP (R28h – R29h)

Reg#	R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R28h	W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0
R29h	W	1	1	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0

When OTP is access, these registers must be set accordantly.

OTP programming sequence

<table>
<tr><th>Step</th><th>Operation</th></tr>
<tr><td>1</td><td>Power up the module with VCI and VDDIO set to customer application input voltage
Turn on the display as normal to 65k/262k color mode (displaying a test pattern if any).</td></tr>
<tr><td>2</td><td>Set nOTP to “1” (R1Eh) and optimizes VcomH by adjusting VCM[5:0] (R1Eh).</td></tr>
<tr><td>3</td><td>Apply Display off sequence (Section 16.2)</td></tr>
<tr><td>4</td><td>Power up the module with VCI and VDDIO set to customer application input voltage
Turn on the display as normal to 65k/262k color mode</td></tr>
<tr><td>5</td><td>Write below commands for OTP initialization and wait for 200ms for activate the OTP :
<table>
<tr><th>Index</th><th>Value</th></tr>
<tr><td>R00h</td><td>0x0001</td></tr>
<tr><td>R28h</td><td>0x0006</td></tr>
<tr><td>R29h</td><td>0x80C0</td></tr>
</table>
Connect a 15.0V (Range of Vpp=14.5V-15.0V) supply to VGH through a current limiting resistor, see figure below.</td></tr>
<tr><td>6</td><td>Write the optimized value found in Step 2 to VCM[5:0] (R1Eh) and set nOTP to “1”.</td></tr>
<tr><td>7</td><td>Fire the OTP by write HEX code “000Ah” to register R28h.</td></tr>
<tr><td>8</td><td>Wait 500ms.</td></tr>
</table>

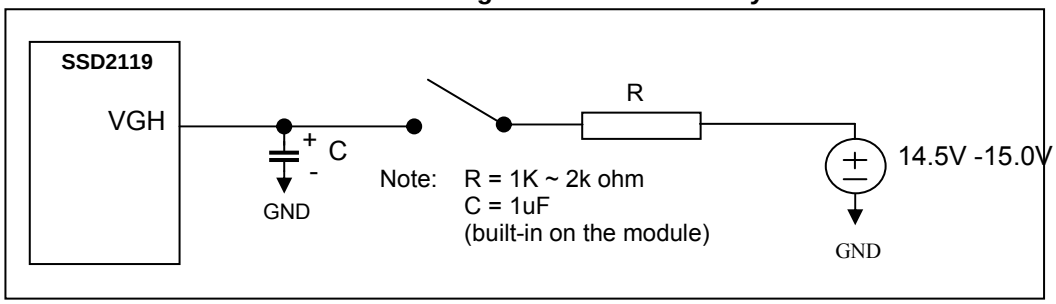
9	OTP complete. Apply Display off sequence and disconnect power

Note: nOTP must set to "0" to activate the OTP effect.
During Step 5 to 9, display is not on
It is possible to skip step3 and step4

Precaution:

1. All capacitors on OTP machine should be discharged completely before placing the LCD module.
2. The OTP programming voltage should not be applied when placing and removing the LCD module.
3. The OTP programming voltage should not be applied before VDDIO/VDDEXT/VCI.
4. After OTP is finished, the capacitors at VGH and VCIX2 must be discharged completely before removing the LCD module.

Figure 9-3: OTP circuitry



Gamma Control (R30h to R3Bh)

Reg#	R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R30h	W	1	0	0	0	0	0	PKP 12	PKP 11	PKP 10	0	0	0	0	0	PKP 02	PKP 01	PKP 00
R31h	W	1	0	0	0	0	0	PKP 32	PKP 31	PKP 30	0	0	0	0	0	PKP 22	PKP 21	PKP 20
R32h	W	1	0	0	0	0	0	PKP 52	PKP 51	PKP 50	0	0	0	0	0	PKP 42	PKP 41	PKP 40
R33h	W	1	0	0	0	0	0	PRP 12	PRP 11	PRP 10	0	0	0	0	0	PRP 02	PRP 01	PRP 00
R34h	W	1	0	0	0	0	0	PKN 12	PKN 11	PKN 10	0	0	0	0	0	PKN 02	PKN 01	PKN 00
R35h	W	1	0	0	0	0	0	PKN 32	PKN 31	PKN 30	0	0	0	0	0	PKN 22	PKN 21	PKN 20
R36h	W	1	0	0	0	0	0	PKN 52	PKN 51	PKN 50	0	0	0	0	0	PKN 42	PKN 41	PKN 40
R37h	W	1	0	0	0	0	0	PRN 12	PRN 11	PRN 10	0	0	0	0	0	PRN 02	PRN 01	PRN 00
R3Ah	W	1	0	0	0	VRP 14	VRP 13	VRP 12	VRP 11	VRP 10	0	0	0	0	VRP 03	VRP 02	VRP 01	VRP 00
R3Bh	W	1	0	0	0	VRN 14	VRN 13	VRN 12	VRN 11	VRN 10	0	0	0	0	VRN 03	VRN 02	VRN 01	VRN 00

Note: please refer to table 5 for POR values.

PKP[52:00]: Gamma micro adjustment register for the positive polarity output

PRP[12:00]: Gradient adjustment register for the positive polarity output

VRP[14:00]: Adjustment register for amplification adjustment of the positive polarity output

PKN[52:00]: Gamma micro adjustment register for the negative polarity output

PRN[12:00]: Gradient adjustment register for the negative polarity output

VRN[14:00]: Adjustment register for the amplification adjustment of the negative polarity output.
(For details, see the Section 11 Gamma Adjustment Function).

Vertical Scroll Control (R41h-R42h) (POR =0000h)

Reg#	R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R41h	W	1	0	0	0	0	0	0	0	VL18	VL17	VL16	VL15	VL14	VL13	VL12	VL11	VL10
	POR		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R42h	W	1	0	0	0	0	0	0	0	VL28	VL27	VL26	VL25	VL24	VL23	VL22	VL21	VL20
	POR		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

VL1[8:0]: Specify scroll length at the scroll display for vertical smooth scrolling. Any raster-row from the first to 240th can be scrolled for the number of the raster-row. After 240th raster-row is displayed, the display restarts from the first raster-row. The display-start raster-row (VL1[8:0]) is valid when VLE1 = "1" or VLE2 = "1". The raster-row display is fixed when VLE[2:1] = "00".

VL2[8:0]: Specify scroll length at the scroll display for vertical smooth scrolling at 2nd screen. The display-start raster-row (VL2[8:0]) is valid when VLE1 = "1" and VLE2 = "1".

Vertical RAM address position (R44h) (POR = EF00h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	VEA7	VEA6	VEA5	VEA4	VEA3	VEA2	VEA1	VEA0	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0
POR		1	1	1	0	1	1	1	1	0	0	0	0	0	0	0	0

VEA[7:0]/VSA[7:0]: Specify the start/end positions of the window address in the vertical direction by an address unit. Data are written to the GDDRAM within the area determined by the addresses specified by VEA[7:0] and VSA[7:0]. These addresses must be set before the RAM write. In setting these bits, make sure that "00"h ≤ VSA[7:0] ≤ VEA[7:0] ≤ "EF"h.

Horizontal RAM address position (R45h-R46h)

Reg#	R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R45h	W	1	0	0	0	0	0	0	0	HSA8	HSA7	HSA6	HSA5	HSA4	HSA3	HSA2	HSA1	HSA0
	POR		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R46h	W	1	0	0	0	0	0	0	0	HEA8	HEA7	HEA6	HEA5	HEA4	HEA3	HEA2	HEA1	HEA0
	POR		0	0	0	0	0	0	0	1	0	0	1	1	1	1	1	1

HSA[8:0]/HEA[8:0]: Specify the start/end positions of the window address in the horizontal direction by an address unit. Data are written to the GRAM within the area determined by the addresses specified by HEA[8:0] and HSA[8:0]. These addresses must be set before the RAM write. In setting these bits, make sure that "00"h ≤ HSA[8:0] ≤ HEA[8:0] ≤ "13F"h.

1st Screen driving position (R48h-R49h)

Reg#	R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R48h	W	1	0	0	0	0	0	0	0	SS18	SS17	SS16	SS15	SS14	SS13	SS12	SS11	SS10
	POR		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R49h	W	1	0	0	0	0	0	0	0	SE18	SE17	SE16	SE15	SE14	SE13	SE12	SE11	SE10
	POR		0	0	0	0	0	0	0	0	1	1	1	0	1	1	1	1

SS1[8:0]: Specify the driving start position for the first screen in a line unit. The LCD driving starts from the set gate driver, i.e. the first driving Gate is G1 if SS1[8:0] = 00H

SE1[8:0]: Specify the driving end position for the first screen in a line unit. The LCD driving is performed to the set gate driver. For instance, when SS1[8:0] = "07"H and SE1[8:0] = "10"H are set, the LCD driving is performed from G7 to G16, and non-selection driving is performed for G1 to G6, G17, and others. Ensure that SS1[8:0] ≤ SE1[8:0] ≤ EFH.

2nd Screen driving position (R4Ah-R4Bh)

Reg#	R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R4Ah	W	1	0	0	0	0	0	0	0	SS28	SS27	SS26	SS25	SS24	SS23	SS22	SS21	SS20
	POR		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R4Bh	W	1	0	0	0	0	0	0	0	SE28	SE27	SE26	SE25	SE24	SE23	SE22	SE21	SE20
	POR		0	0	0	0	0	0	0	0	1	1	1	0	1	1	1	1

SS2[8:0]: Specify the driving start position for the second screen in a line unit. The LCD driving starts from the set gate driver. The second screen is driven when SPT = "1".

SE2[8:0]: Specify the driving end position for the second screen in a line unit. The LCD driving is performed to the set gate driver. For instance, when SPT = "1", SS2[8:0] = "20"H, and SE2[8:0] = "2F"H are set, the LCD driving is performed from G32 to G47. Ensure that SS1[8:0] ≤ SE1[8:0] ; SS2[8:0] ≤ SE2[8:0] ≤ EFH..

RAM address set (R4Eh-R4Fh)

Reg#	R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R4Eh	W	1	0	0	0	0	0	0	0	XAD8	XAD7	XAD6	XAD5	XAD4	XAD 3	XAD 2	XAD 1	XAD 0
	POR		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R4Fh	W	1	0	0	0	0	0	0	0	0	YAD7	YAD6	YAD5	YAD4	YAD3	YAD2	YAD1	YAD0
	POR		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

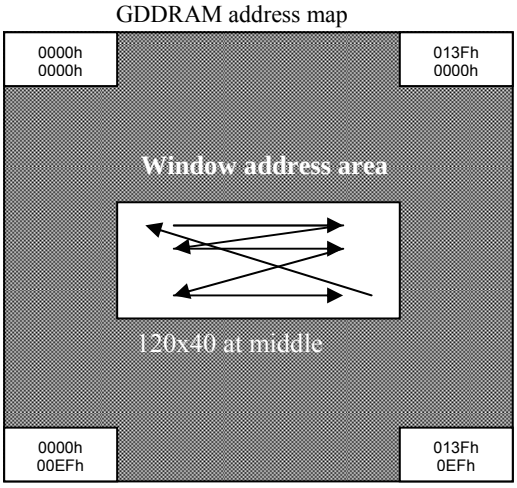
YAD[7:0]: Make initial settings for the GDDRAM Y address in the address counter (AC).
XAD[8:0]: Make initial settings for the GDDRAM X address in the address counter (AC).

After GDDRAM data are written, the address counter is automatically updated according to the settings with AM, I/D bits and setting for a new GDDRAM address is not required in the address counter. Therefore, data are written consecutively without setting an address. The address counter is not automatically updated when data are read out from the GDDRAM. GDDRAM address setting cannot be made during the standby mode. The address setting should be made within the area designated with window addresses.

Window Address Function

The window address function enables writing display data sequentially in a window address area made in the internal GDDRAM. The window address area is made by setting the horizontal address register (start: HSA8-0, end: HEA 8-0 bits) and the vertical address register (start: VSA7-0, end: VEA7-0 bits). The AM and ID[1:0] bits set the transition direction of RAM address (either increment or decrement, horizontal or vertical, respectively). Setting these bits enables the SSD2119 to write data including image data sequentially without taking the data wrap position into account. The window address area must be made within the GDDRAM address map area.

Condition:
00h ≤ HSA[8:0] ≤ HEA[8:0] ≤ 13Fh
00h ≤ VSA[7:0] ≤ VEA[7:0] ≤ EFh
AM and ID[1:0] refer to R11h

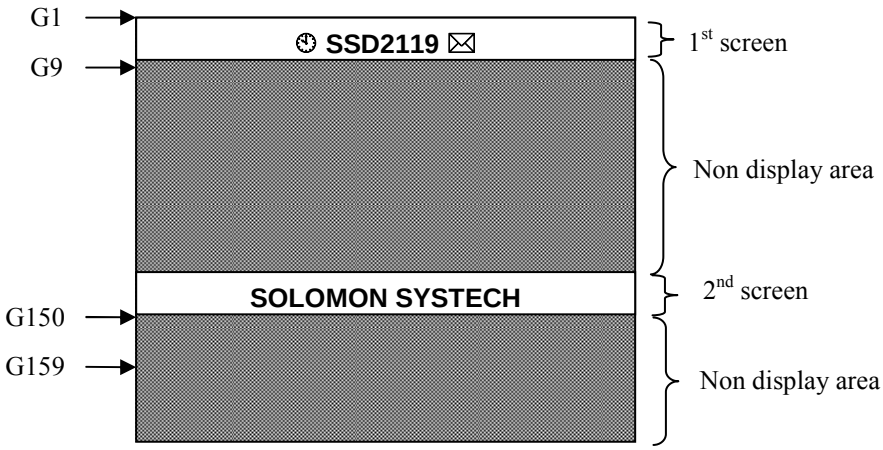


Window address setting area:
HSA[8:0] = 3Bh; HEA[8:0] = B3h
VSA[7:0] = 8Bh; VEA[7:0] = B3h
AM = "0" and ID[1;]] = "11"

Partial Display Mode

The SSD2119 enables to selectively drive two screens at arbitrary positions with the screen-driving position registers (R48h to R4Bh). Only the lines required to display two screens at arbitrary positions are selectively driven to reduce the power consumption.
The first screen driving position registers (R48 and R49) specifies the start line (SS18-10) and the end line (SE18-10) for displaying the first screen. The second screen driving position register (R4A) specifies the start line (SS28-20) and the end line (SE28-20) for displaying the second screen. The second screen control is effective when the SPT bit is set to 1. The total number of lines driven for displaying the first and second screens must be less than the number of lines to drive the LCD.

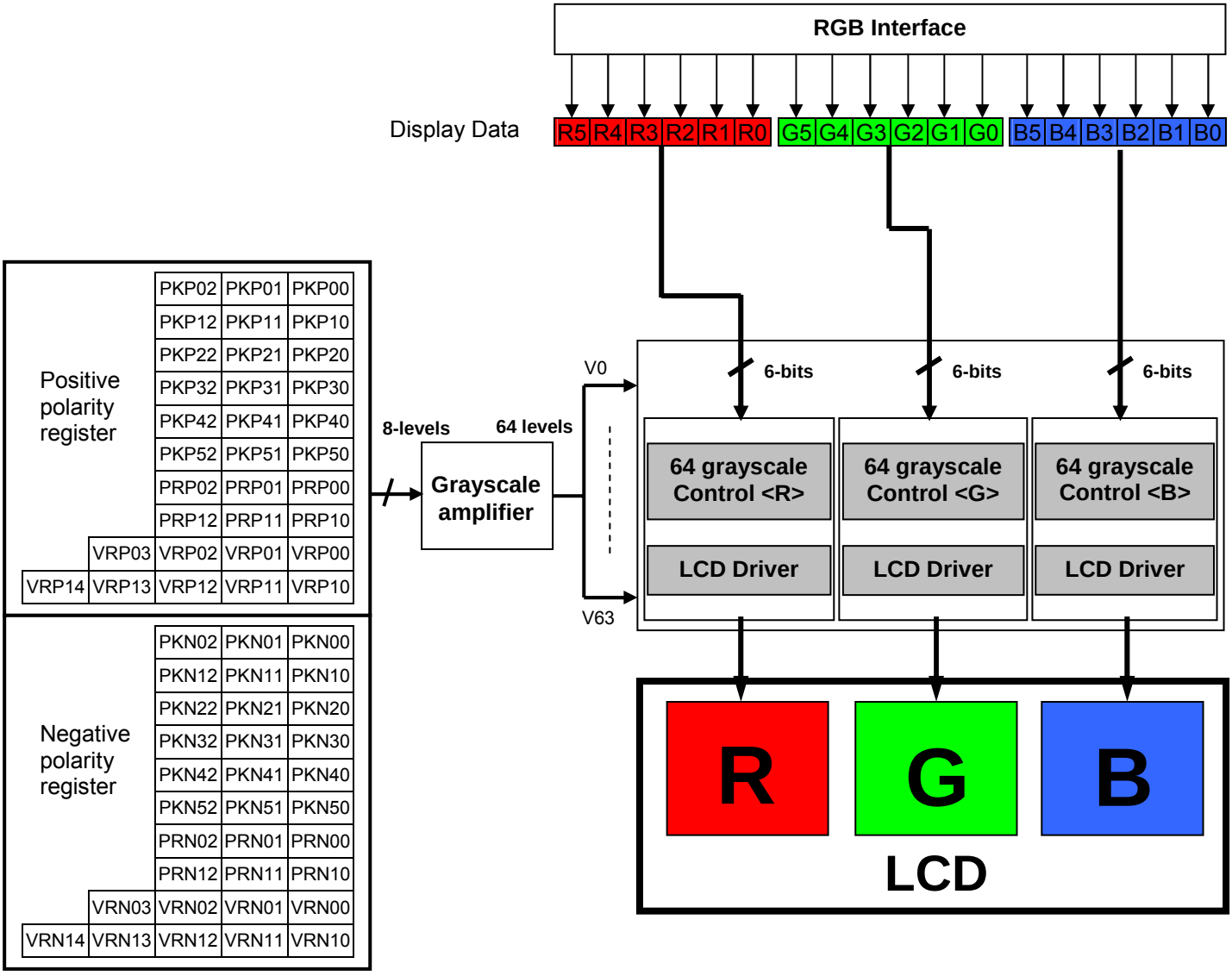
Condition:
SS1[8:0] ≤ SE1[8:0] ≤ EFH
SS1[8:0] ≤ SE1[8:0]
SS2[8:0] ≤ SE2[8:0] ≤ EFH



The number of driven display lines: MUX[8:0] = 13F (319+1 lines)
1st screen setting: SS[18:10] = 00h, SE[18:10] = 09h
2nd screen seeting: SS[28:10] = 96h, SE[28:10] = 9Fh

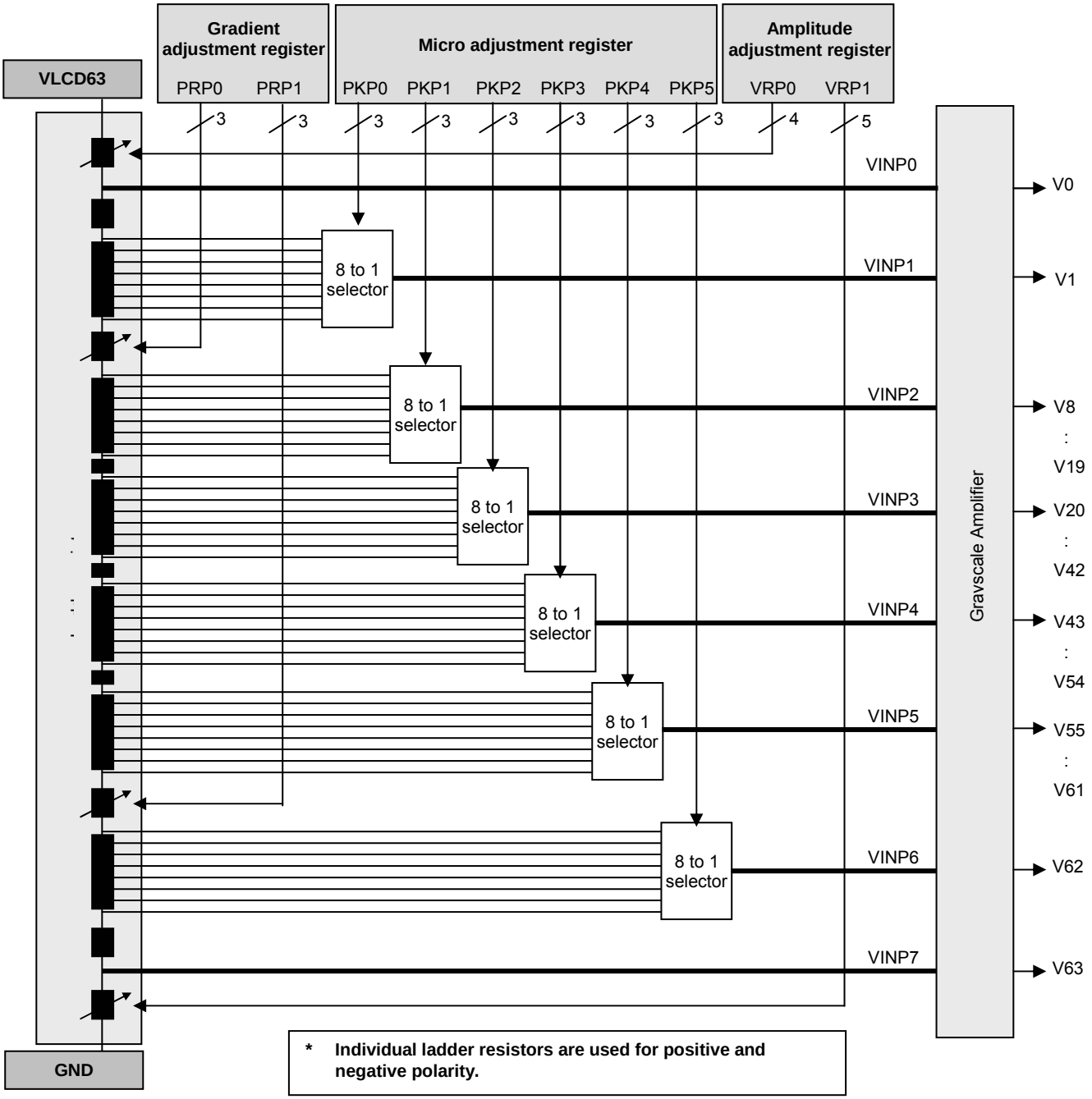
10 GAMMA ADJUSTMENT FUNCTION

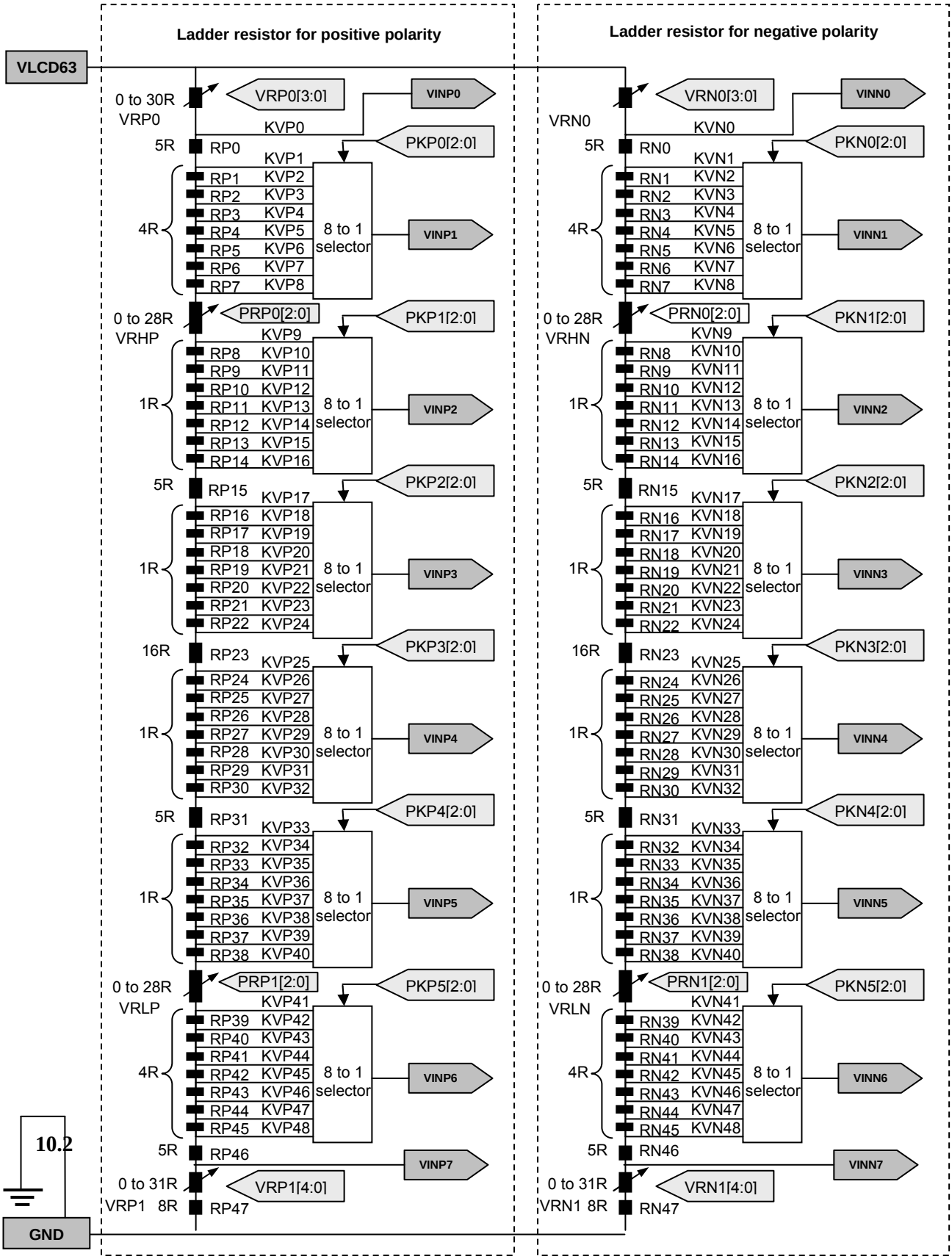
The SSD2119 incorporates gamma adjustment function for the 262,144-color display. Gamma adjustment is implemented by deciding the 8-grayscale levels with angle adjustment and micro adjustment register. Also, angle adjustment and micro adjustment is fixed for each of the internal positive and negative polarity. Set up by the liquid crystal panel's specification.



10.1 Structure of Grayscale Amplifier

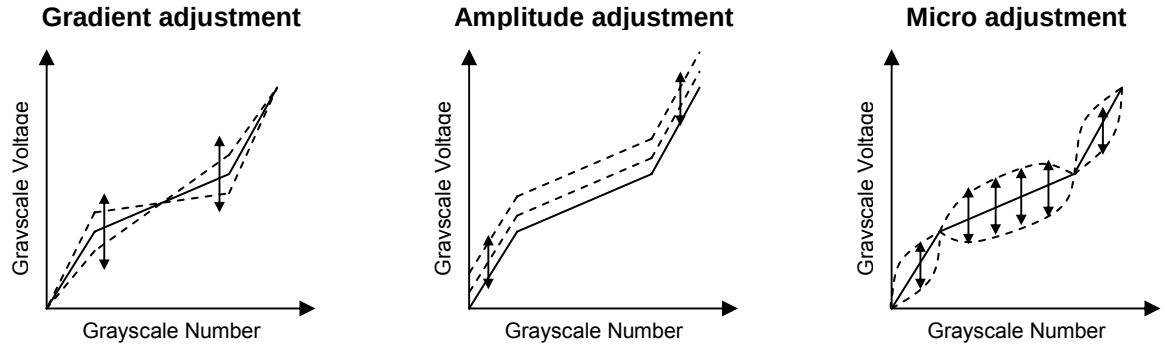
Below figure indicates the structure of the grayscale amplifier. It determines 8 levels (VIN0-VIN7) by the gradient adjuster and the micro adjustment register. Also, dividing these levels with ladder resistors generates V0 to V63.




Ladder resistor for positive polarity
Ladder resistor for negative polarity
VLCD63
0 to 30R
VRP0
5R
4R
1R
16R
0 to 28R
VRHP
VRLP
0 to 31R
VRP1 8R
VRN0
VRHN
VRLN
VRP0[3:0]
VRN0[3:0]
VRP1[4:0]
VRN1[4:0]
PRP0[2:0]
PRP1[2:0]
PRN0[2:0]
PRN1[2:0]
RP0
RP1
RP2
RP3
RP4
RP5
RP6
RP7
RP8
RP9
RP10
RP11
RP12
RP13
RP14
RP15
RP16
RP17
RP18
RP19
RP20
RP21
RP22
RP23
RP24
RP25
RP26
RP27
RP28
RP29
RP30
RP31
RP32
RP33
RP34
RP35
RP36
RP37
RP38
RP39
RP40
RP41
RP42
RP43
RP44
RP45
RP46
RP47
RN0
RN1
RN2
RN3
RN4
RN5
RN6
RN7
RN8
RN9
RN10
RN11
RN12
RN13
RN14
RN15
RN16
RN17
RN18
RN19
RN20
RN21
RN22
RN23
RN24
RN25
RN26
RN27
RN28
RN29
RN30
RN31
RN32
RN33
RN34
RN35
RN36
RN37
RN38
RN39
RN40
RN41
RN42
RN43
RN44
RN45
RN46
RN47
KVP0
KVP1
KVP2
KVP3
KVP4
KVP5
KVP6
KVP7
KVP8
KVP9
KVP10
KVP11
KVP12
KVP13
KVP14
KVP15
KVP16
KVP17
KVP18
KVP19
KVP20
KVP21
KVP22
KVP23
KVP24
KVP25
KVP26
KVP27
KVP28
KVP29
KVP30
KVP31
KVP32
KVP33
KVP34
KVP35
KVP36
KVP37
KVP38
KVP39
KVP40
KVP41
KVP42
KVP43
KVP44
KVP45
KVP46
KVP47
KVP48
KVN0
KVN1
KVN2
KVN3
KVN4
KVN5
KVN6
KVN7
KVN8
KVN9
KVN10
KVN11
KVN12
KVN13
KVN14
KVN15
KVN16
KVN17
KVN18
KVN19
KVN20
KVN21
KVN22
KVN23
KVN24
KVN25
KVN26
KVN27
KVN28
KVN29
KVN30
KVN31
KVN32
KVN33
KVN34
KVN35
KVN36
KVN37
KVN38
KVN39
KVN40
KVN41
KVN42
KVN43
KVN44
KVN45
KVN46
KVN47
KVN48
8 to 1 selector
PKP0[2:0]
PKP1[2:0]
PKP2[2:0]
PKP3[2:0]
PKP4[2:0]
PKP5[2:0]
PKN0[2:0]
PKN1[2:0]
PKN2[2:0]
PKN3[2:0]
PKN4[2:0]
PKN5[2:0]
VINP0
VINP1
VINP2
VINP3
VINP4
VINP5
VINP6
VINP7
VINN0
VINN1
VINN2
VINN3
VINN4
VINN5
VINN6
VINN7
10.2
GND

Gamma Adjustment Register

This block is the register to set up the grayscale voltage adjusting to the gamma specification of the LCD panel. This register can independent set up to positive/negative polarities and there are three types of register groups to adjust gradient, amplitude, and micro-adjustment on number of the grayscale, characteristics of the grayscale voltage. (Using the same setting for Reference-value and R.G.B.) Following graphics indicates the operation of each adjusting register.



10.2.1 Gradient adjusting register

The gradient-adjusting resistor is to adjust around middle gradient, specification of the grayscale number and the grayscale voltage without changing the dynamic range. To accomplish the adjustment, it controls the variable resistors in the middle of the ladder resistor by registers (PRP(N)0 / PRP(N)1) for the grayscale voltage generator. Also, there is an independent resistor on the positive/negative polarities in order for corresponding to asymmetry drive.

10.2.2 Amplitude adjusting register

The amplitude-adjusting resistor is to adjust amplitude of the grayscale voltage. To accomplish the adjustment, it controls the variable resistors in the boundary of the ladder resistor by registers (VRP(N)0 / VRP(N)1) for the grayscale voltage generator. Also, there is an independent resistor on the positive/negative polarities as well as the gradient-adjusting resistor.

10.2.3 Micro adjusting register

The micro-adjusting register is to make subtle adjustment of the grayscale voltage level. To accomplish the adjustment, it controls each reference voltage level by the 8 to 1 selector towards the 8-level reference voltage generated from the ladder resistor. Also, there is an independent resistor on the positive/negative polarities as well as other adjusting resistors.

10.3 Ladder Resistor / 8 to 1 selector

This block outputs the reference voltage of the grayscale voltage. There are two ladder resistors including the variable resistor and the 8 to 1 selector selecting voltage generated by the ladder resistor. The gamma registers control the variable resistors and 8 to 1 selector resistors.

Variable Resistor

There are 3 types of the variable resistors that are for the gradient and amplitude adjustment. The resistance is set by the resistor (PRP(N)0 / PRP(N)1) and (VRP(N)0 / VRP(N)1) as below.

PRP(N)[0:1]	Resistance
000	0R
001	4R
010	8R
011	12R
100	16R
101	20R
110	24R
111	28R

VRP(N)0	Resistance
0000	0R
0001	2R
0010	4R
: Step = 2R :	
1110	28R
1111	30R

VRP(N)1	Resistance
00000	0R
00001	1R
00010	2R
: Step = 1R :	
11110	30R
11111	31R

8 to 1 selecter

In the 8 to 1 selector, a reference voltage VIN can be selected from the levels which are generated by the ladder resistors. There are six types of reference voltage (VIN1 to VIN6) and totally 48 divided voltages can be selected in one ladder resistor. Following figure explains the relationship between the micro-adjusting register and the selecting voltage.

Postive polarity							Negative polarity						
Registor	Selected voltage						Registor	Selected voltage					
PKP[2:0]	VINP1	VINP2	VINP3	VINP4	VINP5	VINP6	PKN[2:0]	VINN1	VINN2	VINN3	VINN4	VINN5	VINN6
000	KVP1	KVP9	KVP17	KVP25	KVP33	KVP41	000	KVN1	KVN9	KVN17	KVN25	KVN33	KVN41
001	KVP2	KVP10	KVP18	KVP26	KVP34	KVP42	001	KVN2	KVN10	KVN18	KVN26	KVN34	KVN42
010	KVP3	KVP11	KVP19	KVP27	KVP35	KVP43	010	KVN3	KVN11	KVN19	KVN27	KVN35	KVN43
011	KVP4	KVP12	KVP20	KVP28	KVP36	KVP44	011	KVN4	KVN12	KVN20	KVN28	KVN36	KVN44
100	KVP5	KVP13	KVP21	KVP29	KVP37	KVP45	100	KVN5	KVN13	KVN21	KVN29	KVN37	KVN45
101	KVP6	KVP14	KVP22	KVP30	KVP38	KVP46	101	KVN6	KVN14	KVN22	KVN30	KVN38	KVN46
110	KVP7	KVP15	KVP23	KVP31	KVP39	KVP47	110	KVN7	KVN15	KVN23	KVN31	KVN39	KVN47
111	KVP8	KVP16	KVP24	KVP32	KVP40	KVP48	111	KVN8	KVN16	KVN24	KVN32	KVN40	KVN48

Grayscale voltage	Formula	Grayscale voltage	Formula	Grayscale voltage	Formula
V0	VINP(N)0	V22	V43+(V20-V43)*(21/23)	V44	V55+(V43-V55)*(22/24)
V1	VINP(N)1	V23	V43+(V20-V43)*(20/23)	V45	V55+(V43-V55)*(20/24)
V2	V8+(V1-V8)*(30/48)	V24	V43+(V20-V43)*(19/23)	V46	V55+(V43-V55)*(18/24)
V3	V8+(V1-V8)*(23/48)	V25	V43+(V20-V43)*(18/23)	V47	V55+(V43-V55)*(16/24)
V4	V8+(V1-V8)*(16/48)	V26	V43+(V20-V43)*(17/23)	V48	V55+(V43-V55)*(14/24)
V5	V8+(V1-V8)*(12/48)	V27	V43+(V20-V43)*(16/23)	V49	V55+(V43-V55)*(12/24)
V6	V8+(V1-V8)*(8/48)	V28	V43+(V20-V43)*(15/23)	V50	V55+(V43-V55)*(10/24)
V7	V8+(V1-V8)*(4/48)	V29	V43+(V20-V43)*(14/23)	V51	V55+(V43-V55)*(8/24)
V8	VINP(N)2	V30	V43+(V20-V43)*(13/23)	V52	V55+(V43-V55)*(6/24)
V9	V20+(V8-V20)*(22/24)	V31	V43+(V20-V43)*(12/23)	V53	V55+(V43-V55)*(4/24)
V10	V20+(V8-V20)*(20/24)	V32	V43+(V20-V43)*(11/23)	V54	V55+(V43-V55)*(2/24)
V11	V20+(V8-V20)*(18/24)	V33	V43+(V20-V43)*(10/23)	V55	VINP(N)5
V12	V20+(V8-V20)*(16/24)	V34	V43+(V20-V43)*(9/23)	V56	V62+(V55-V62)*(44/48)
V13	V20+(V8-V20)*(14/24)	V35	V43+(V20-V43)*(8/23)	V57	V62+(V55-V62)*(40/48)
V14	V20+(V8-V20)*(12/24)	V36	V43+(V20-V43)*(7/23)	V58	V62+(V55-V62)*(36/48)
V15	V20+(V8-V20)*(10/24)	V37	V43+(V20-V43)*(6/23)	V59	V62+(V55-V62)*(32/48)
V16	V20+(V8-V20)*(8/24)	V38	V43+(V20-V43)*(5/23)	V60	V62+(V55-V62)*(25/48)
V17	V20+(V8-V20)*(6/24)	V39	V43+(V20-V43)*(4/23)	V61	V62+(V55-V62)*(18/48)
V18	V20+(V8-V20)*(4/24)	V40	V43+(V20-V43)*(3/23)	V62	VINP(N)6
V19	V20+(V8-V20)*(2/24)	V41	V43+(V20-V43)*(2/23)	V63	VINP(N)7
V20	VINP(N)3	V42	V43+(V20-V43)*(1/23)		
V21	V43+(V20-V43)*(22/23)	V43	VINP(N)4		

Reference voltage of positive polarity:

Reference	Formula	Micr0-adjusting rgister	Reference voltage
KVP0	VLCD63 - ΔV x VRP0 / SUMRP	--	VINP0
KVP1	VLCD63 - ΔV x (VRP0 + 5R) / SUMRP	PKP0[2:0] = “000”	VINP1
KVP2	VLCD63 - ΔV x (VRP0 + 9R) / SUMRP	PKP0[2:0] = “001”	
KVP3	VLCD63 - ΔV x (VRP0 + 13R) / SUMRP	PKP0[2:0] = “010”	
KVP4	VLCD63 - ΔV x (VRP0 + 17R) / SUMRP	PKP0[2:0] = “011”	
KVP5	VLCD63 - ΔV x (VRP0 + 21R) / SUMRP	PKP0[2:0] = “100”	
KVP6	VLCD63 - ΔV x (VRP0 + 25R) / SUMRP	PKP0[2:0] = “101”	
KVP7	VLCD63 - ΔV x (VRP0 + 29R) / SUMRP	PKP0[2:0] = “110”	
KVP8	VLCD63 - ΔV x (VRP0 + 33R) / SUMRP	PKP0[2:0] = “111”	
KVP9	VLCD63 - ΔV x (VRP0 + 33R + VRHP) / SUMRP	PKP1[2:0] = “000”	VINP2
KVP10	VLCD63 - ΔV x (VRP0 + 34R + VRHP) / SUMRP	PKP1[2:0] = “001”	
KVP11	VLCD63 - ΔV x (VRP0 + 35R + VRHP) / SUMRP	PKP1[2:0] = “010”	
KVP12	VLCD63 - ΔV x (VRP0 + 36R + VRHP) / SUMRP	PKP1[2:0] = “011”	
KVP13	VLCD63 - ΔV x (VRP0 + 37R + VRHP) / SUMRP	PKP1[2:0] = “100”	
KVP14	VLCD63 - ΔV x (VRP0 + 38R + VRHP) / SUMRP	PKP1[2:0] = “101”	
KVP15	VLCD63 - ΔV x (VRP0 + 39R + VRHP) / SUMRP	PKP1[2:0] = “110”	
KVP16	VLCD63 - ΔV x (VRP0 + 40R + VRHP) / SUMRP	PKP1[2:0] = “111”	
KVP17	VLCD63 - ΔV x (VRP0 + 45R + VRHP) / SUMRP	PKP2[2:0] = “000”	VINP3
KVP18	VLCD63 - ΔV x (VRP0 + 46R + VRHP) / SUMRP	PKP2[2:0] = “001”	
KVP19	VLCD63 - ΔV x (VRP0 + 47R + VRHP) / SUMRP	PKP2[2:0] = “010”	
KVP20	VLCD63 - ΔV x (VRP0 + 48R + VRHP) / SUMRP	PKP2[2:0] = “011”	
KVP21	VLCD63 - ΔV x (VRP0 + 49R + VRHP) / SUMRP	PKP2[2:0] = “100”	
KVP22	VLCD63 - ΔV x (VRP0 + 50R + VRHP) / SUMRP	PKP2[2:0] = “101”	
KVP23	VLCD63 - ΔV x (VRP0 + 51R + VRHP) / SUMRP	PKP2[2:0] = “110”	
KVP24	VLCD63 - ΔV x (VRP0 + 52R + VRHP) / SUMRP	PKP2[2:0] = “111”	
KVP25	VLCD63 - ΔV x (VRP0 + 68R + VRHP) / SUMRP	PKP3[2:0] = “000”	VINP4
KVP26	VLCD63 - ΔV x (VRP0 + 69R + VRHP) / SUMRP	PKP3[2:0] = “001”	
KVP27	VLCD63 - ΔV x (VRP0 + 70R + VRHP) / SUMRP	PKP3[2:0] = “010”	
KVP28	VLCD63 - ΔV x (VRP0 + 71R + VRHP) / SUMRP	PKP3[2:0] = “011”	
KVP29	VLCD63 - ΔV x (VRP0 + 72R + VRHP) / SUMRP	PKP3[2:0] = “100”	
KVP30	VLCD63 - ΔV x (VRP0 + 73R + VRHP) / SUMRP	PKP3[2:0] = “101”	
KVP31	VLCD63 - ΔV x (VRP0 + 74R + VRHP) / SUMRP	PKP3[2:0] = “110”	
KVP32	VLCD63 - ΔV x (VRP0 + 75R + VRHP) / SUMRP	PKP3[2:0] = “111”	
KVP33	VLCD63 - ΔV x (VRP0 + 80R + VRHP) / SUMRP	PKP4[2:0] = “000”	VINP5
KVP34	VLCD63 - ΔV x (VRP0 + 81R + VRHP) / SUMRP	PKP4[2:0] = “001”	
KVP35	VLCD63 - ΔV x (VRP0 + 82R + VRHP) / SUMRP	PKP4[2:0] = “010”	
KVP36	VLCD63 - ΔV x (VRP0 + 83R + VRHP) / SUMRP	PKP4[2:0] = “011”	
KVP37	VLCD63 - ΔV x (VRP0 + 84R + VRHP) / SUMRP	PKP4[2:0] = “100”	
KVP38	VLCD63 - ΔV x (VRP0 + 85R + VRHP) / SUMRP	PKP4[2:0] = “101”	
KVP39	VLCD63 - ΔV x (VRP0 + 86R + VRHP) / SUMRP	PKP4[2:0] = “110”	
KVP40	VLCD63 - ΔV x (VRP0 + 87R + VRHP) / SUMRP	PKP4[2:0] = “111”	
KVP41	VLCD63 - ΔV x (VRP0 + 87R + VRHP + VRLP) / SUMRP	PKP5[2:0] = “000”	VINP6
KVP42	VLCD63 - ΔV x (VRP0 + 91R + VRHP + VRLP) / SUMRP	PKP5[2:0] = “001”	
KVP43	VLCD63 - ΔV x (VRP0 + 95R + VRHP + VRLP) / SUMRP	PKP5[2:0] = “010”	
KVP44	VLCD63 - ΔV x (VRP0 + 99R + VRHP + VRLP) / SUMRP	PKP5[2:0] = “011”	
KVP45	VLCD63 - ΔV x (VRP0 + 103R + VRHP + VRLP) / SUMRP	PKP5[2:0] = “100”	
KVP46	VLCD63 - ΔV x (VRP0 + 107R + VRHP + VRLP) / SUMRP	PKP5[2:0] = “101”	
KVP47	VLCD63-ΔV x (VRP0 + 111R + VRHP + VRLP) / SUMRP	PKP5[2:0] = “110”	
KVP48	VLCD63 - ΔV x (VRP0 + 115R + VRHP + VRLP) / SUMRP	PKP5[2:0] = “111”	
KVP49	VLCD63 - ΔV x (VRP0 + 120R + VRHP + VRLP) / SUMRP	--	VINP7

SUMRP: Total of the positive polarity ladder resistance = 128R + VRHP + VRLP + VRP0 + VRP1

ΔV: Voltage difference between VLCD63 and of GND.

Reference voltage of negative polarity:

Reference	Formula	Micr0-adjusting rgister	Reference voltage
KVN0	VLCD63 - ΔV x VRN0 / SUMRN	--	VINN0
KVN1	VLCD63 - ΔV x (VRN0 + 5R) / SUMRN	PKN0[2:0] = “000”	VINN1
KVN2	VLCD63 - ΔV x (VRN0 + 9R) / SUMRN	PKN0[2:0] = “001”	
KVN3	VLCD63 - ΔV x (VRN0 + 13R) / SUMRN	PKN0[2:0] = “010”	
KVN4	VLCD63 - ΔV x (VRN0 + 17R) / SUMRN	PKN0[2:0] = “011”	
KVN5	VLCD63 - ΔV x (VRN0 + 21R) / SUMRN	PKN0[2:0] = “100”	
KVN6	VLCD63 - ΔV x (VRN0 + 25R) / SUMRN	PKN0[2:0] = “101”	
KVN7	VLCD63 - ΔV x (VRN0 + 29R) / SUMRN	PKN0[2:0] = “110”	
KVN8	VLCD63 - ΔV x (VRN0 + 33R) / SUMRN	PKN0[2:0] = “111”	
KVN9	VLCD63 - ΔV x (VRN0 + 33R + VRHN) / SUMRN	PKN1[2:0] = “000”	VINN2
KVN10	VLCD63 - ΔV x (VRN0 + 34R + VRHN) / SUMRN	PKN1[2:0] = “001”	
KVN11	VLCD63 - ΔV x (VRN0 + 35R + VRHN) / SUMRN	PKN1[2:0] = “010”	
KVN12	VLCD63 - ΔV x (VRN0 + 36R + VRHN) / SUMRN	PKN1[2:0] = “011”	
KVN13	VLCD63 - ΔV x (VRN0 + 37R + VRHN) / SUMRN	PKN1[2:0] = “100”	
KVN14	VLCD63 - ΔV x (VRN0 + 38R + VRHN) / SUMRN	PKN1[2:0] = “101”	
KVN15	VLCD63 - ΔV x (VRN0 + 39R + VRHN) / SUMRN	PKN1[2:0] = “110”	
KVN16	VLCD63 - ΔV x (VRN0 + 40R + VRHN) / SUMRN	PKN1[2:0] = “111”	
KVN17	VLCD63 - ΔV x (VRN0 + 45R + VRHN) / SUMRN	PKN2[2:0] = “000”	VINN3
KVN18	VLCD63 - ΔV x (VRN0 + 46R + VRHN) / SUMRN	PKN2[2:0] = “001”	
KVN19	VLCD63 - ΔV x (VRN0 + 47R + VRHN) / SUMRN	PKN2[2:0] = “010”	
KVN20	VLCD63 - ΔV x (VRN0 + 48R + VRHN) / SUMRN	PKN2[2:0] = “011”	
KVN21	VLCD63 - ΔV x (VRN0 + 49R + VRHN) / SUMRN	PKN2[2:0] = “100”	
KVN22	VLCD63 - ΔV x (VRN0 + 50R + VRHN) / SUMRN	PKN2[2:0] = “101”	
KVN23	VLCD63 - ΔV x (VRN0 + 51R + VRHN) / SUMRN	PKN2[2:0] = “110”	
KVN24	VLCD63 - ΔV x (VRN0 + 52R + VRHN) / SUMRN	PKN2[2:0] = “111”	
KVN25	VLCD63 - ΔV x (VRN0 + 68R + VRHN) / SUMRN	PKN3[2:0] = “000”	VINN4
KVN26	VLCD63 - ΔV x (VRN0 + 69R + VRHN) / SUMRN	PKN3[2:0] = “001”	
KVN27	VLCD63 - ΔV x (VRN0 + 70R + VRHN) / SUMRN	PKN3[2:0] = “010”	
KVN28	VLCD63 - ΔV x (VRN0 + 71R + VRHN) / SUMRN	PKN3[2:0] = “011”	
KVN29	VLCD63 - ΔV x (VRN0 + 72R + VRHN) / SUMRN	PKN3[2:0] = “100”	
KVN30	VLCD63 - ΔV x (VRN0 + 73R + VRHN) / SUMRN	PKN3[2:0] = “101”	
KVN31	VLCD63 - ΔV x (VRN0 + 74R + VRHN) / SUMRN	PKN3[2:0] = “110”	
KVN32	VLCD63 - ΔV x (VRN0 + 75R + VRHN) / SUMRN	PKN3[2:0] = “111”	
KVN33	VLCD63 - ΔV x (VRN0 + 80R + VRHN) / SUMRN	PKN4[2:0] = “000”	VINN5
KVN34	VLCD63 - ΔV x (VRN0 + 81R + VRHN) / SUMRN	PKN4[2:0] = “001”	
KVN35	VLCD63 - ΔV x (VRN0 + 82R + VRHN) / SUMRN	PKN4[2:0] = “010”	
KVN36	VLCD63 - ΔV x (VRN0 + 83R + VRHN) / SUMRN	PKN4[2:0] = “011”	
KVN37	VLCD63 - ΔV x (VRN0 + 84R + VRHN) / SUMRN	PKN4[2:0] = “100”	
KVN38	VLCD63 - ΔV x (VRN0 + 85R + VRHN) / SUMRN	PKN4[2:0] = “101”	
KVN39	VLCD63 - ΔV x (VRN0 + 86R + VRHN) / SUMRN	PKN4[2:0] = “110”	
KVN40	VLCD63 - ΔV x (VRN0 + 87R + VRHN) / SUMRN	PKN4[2:0] = “111”	
KVN41	VLCD63 - ΔV x (VRN0 + 87R + VRHN + VRLN) / SUMRN	PKN5[2:0] = “000”	VINN6
KVN42	VLCD63 - ΔV x (VRN0 + 91R + VRHN + VRLN) / SUMRN	PKN5[2:0] = “001”	
KVN43	VLCD63 - ΔV x (VRN0 + 95R + VRHN + VRLN) / SUMRN	PKN5[2:0] = “010”	
KVN44	VLCD63 - ΔV x (VRN0 + 99R + VRHN + VRLN) / SUMRN	PKN5[2:0] = “011”	
KVN45	VLCD63 - ΔV x (VRN0 + 103R + VRHN + VRLN) / SUMRN	PKN5[2:0] = “100”	
KVN46	VLCD63 - ΔV x (VRN0 + 107R + VRHN + VRLN) / SUMRN	PKN5[2:0] = “101”	
KVN47	VLCD63-ΔV x (VRN0 + 111R + VRHN + VRLN) / SUMRN	PKN5[2:0] = “110”	
KVN48	VLCD63 - ΔV x (VRN0 + 115R + VRHN + VRLN) / SUMRN	PKN5[2:0] = “111”	
KVN49	VLCD63 - ΔV x (VRN0 + 120R + VRHN + VRLN) / SUMRN	--	VINN7

SUMRN: Total of the negative polarity ladder resistance = 128R + VRHN + VRLN + VRN0 + VRN1

ΔV: Voltage difference between VLCD63 and of GND.

11 MAXIMUM RATINGS

Maximum Ratings (Voltage Referenced to V_{SS})

Symbol	Parameter	Value	Unit
VDDIO	Supply Voltage	-0.3 to +4.0	V
VCI	Input Voltage	VSS - 0.3 to 5.0	V
I	Current Drain Per Pin Excluding V_{DDIO} and V_{SS}	25	mA
T_A	Operating Temperature	-40 to +85	^oC
T_{stg}	Storage Temperature	-65 to +150	^oC

Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section.
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, strong electric fields, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices. It is advised that proper precautions to be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that VCI and Vout be constrained to the range VSS < VDDIO ≤ VCI < V_{OUT}. Reliability of operation is enhanced if unused input is connected to an appropriate logic voltage level (e.g., either VSS or VDDIO). Unused outputs must be left open. This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

12 DC CHARACTERISTICS

DC Characteristics (Unless otherwise specified, Voltage Referenced to V_{SS}, V_{DDIO} = 1.4 to 3.6V, T_A = -40 to 85°C)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
VDDIO	Power supply pin of IO pins	Recommend Operating Voltage Possible Operating Voltage	1.4	-	3.6	V
VCI	Booster Reference Supply Voltage Range	Recommend Operating Voltage Possible Operating Voltage	2.5 or VDDIO whichever is higher	-	3.6	V
VGH	Gate driver High Output Voltage Booster efficiency	No panel loading; 4x or 5x booster; ITO for CYP, CYN, VCIX2, VCI and VCHS = 10 Ohm	88	90	-	%
		No panel loading; 6x booster; ITO for CYP, CYN, VCIX2, VCI and VCHS = 10 Ohm	82	84	-	%
VCIX2	VCIX2 primary booster efficiency	No panel loading, ITO for CYP, CYN, VCIX2, VCI and VCHS = 10 Ohm	83	85	-	%
VGH	Gate driver High Output Voltage		9	-	18	V
VGL	Gate driver Low Output Voltage		-15	-	-6	V
VcomH	Vcom High Output Voltage		V_{CI} + 0.5	-	5	V
VcomL	Vcom Low Output Voltage		$-V_{CIM}$+0.5	-	-1	V
VLCD63	Max. Source Voltage		-	-	6	V
ΔVLCD63	Source voltage variation		-2		2	%
V_{OH1}	Logic High Output Voltage	Iout=-100μA	0.9* VDDIO	-	VDDIO	V
V_{OL1}	Logic Low Output Voltage	Iout=100μA	0	-	0.1*VDDIO	V
V_{IH1}	Logic High Input voltage		0.8*VDDIO	-	VDDIO	V
V_{IL1}	Logic Low Input voltage		0	-	0.2*VDDIO	V
I_{OH}	Logic High Output Current Source	Vout = V_{DDIO}-0.4V	50	-	-	μA
I_{OL}	Logic Low Output Current Drain	Vout = 0.4V	-	-	-50	μA
I_{OZ}	Logic Output Tri-state Current Drain Source		-1	-	1	μA
I_{IL}/I_{IH}	Logic Input Current		-1	-	1	μA

C_{IN}	Logic Pins Input Capacitance			-	5	7.5	pF
R_{SON}	Source drivers output resistance			-	1	-	kΩ
R_{GON}	Gate drivers output resistance			-	500	-	Ω
R_{CON}	Vcom output resistance			-	200	-	Ω
I_{dp}(262k)	Display current for 262k	Vddio= 1.8V, Vci = 2.8V, 5x/-5x(VGH/VGL) booster ratio. Full color current consumption, without panel loading	Ivdd	-	150	300	uA
			Ivci	-	2.5	8	mA
I_{dp}(8 color)	Display current for 8 color mode	Vddio= 1.8V, Vci = 2.8V, +5/-3(VGH/VGL) booster ratio Current consumption for 8 color partial display, without panel loading	Ivdd	-	120	300	µA
			Ivci	-	1	5	mA
I_{halt}	Halt mode current	Oscillator off, no source/gate output, Ram read write halt. RESB pull-low	Ivdd	-	1	2	µA
			Ivci	-	65	120	µA
I_{slp}	Sleep mode current	Oscillator off, no source/gate output, Ram read write halt. Send command R10-0001 (sleep mode)	Ivdd	-	1	2	µA
			Ivci	-	65	200	µA
$I_{deepsleep}$	Deep Sleep mode current	Oscillator off, no source/gate output, Ram read write halt. Send command R10-0001 (sleep mode), R12-6D99 (deep sleep mode)	Ivdd	-	0.5	1	µA
			Ivci	-	5	15	µA

Remark:
Ivdd = Ivddio
Ihalt is the current consumption of Power on and Reset keeps low state; the maximum rating is 100uA.
The setting of VLCD63 is needed to below 0.5V of VCIX2. It is the prevention of VCIX2 noise to couple to VLCD63 gamma voltage.

13 AC CHARACTERISTICS

Table 13-1: Parallel 6800 Timing Characteristics

(T_A = -40 to 85°C, V_{DDIO} = 1.4V to 3.6V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time (write cycle)	75	-	-	ns
t_{cycle}	Clock Cycle Time (read cycle) (Based on VOL/VOH = 0.3*VDDIO/0.7*VDDIO)	450	-	-	ns
t_{AS}	Address Setup Time ($R/\overline{W}$)	0	-	-	ns
t_{AH}	Address Hold Time ($R/\overline{W}$)	0	-	-	ns
t_{DSW}	Data Setup Time (D0~D7, WRITE)	5	-	-	ns
t_{DHW}	Data Hold Time (D0~D7, WRITE))	5	-	-	ns
t_{ACC}	Data Access Time (D0~D7, READ)	250	-	-	ns
t_{OH}	Output Hold time (D0~D7, READ)	100	-	-	ns
PW_{CSL}	Pulse width /CS low (write cycle)	40	-	-	ns
PW_{CSH}	Pulse width /CS high (write cycle)	25	-	-	ns
PW_{CSL}	Pulse width /CS low (read cycle)	500	-	-	ns
PW_{CSH}	Pulse width /CS high (read cycle)	500	-	-	ns
t_R	Rise time	-	-	4	ns
t_F	Fall time	-	-	4	ns

Note: CS can be pulled low during the write cycle, only /RW is needed to be toggled

Figure 13-1: Parallel 6800-series Interface Timing Characteristics

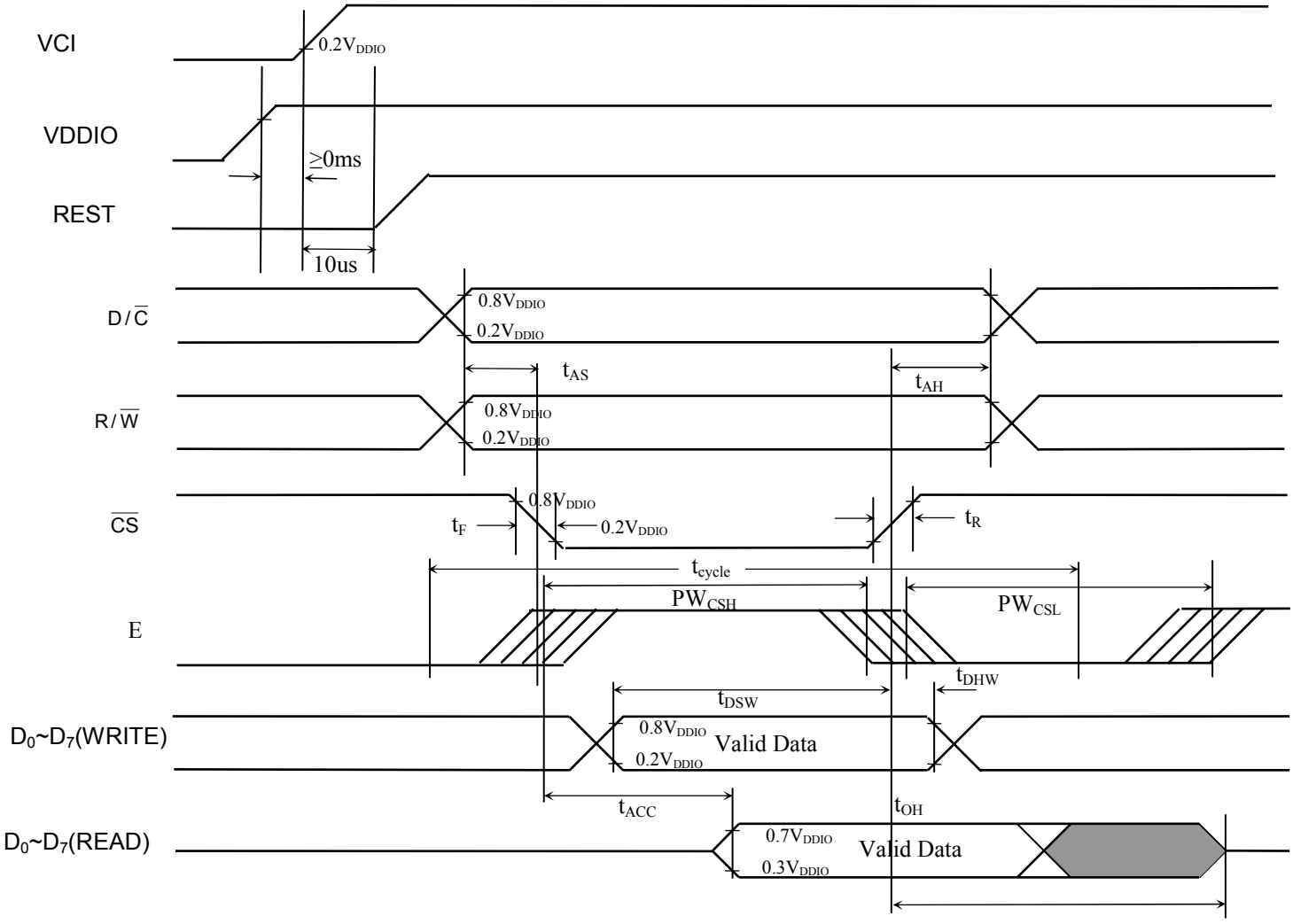


Table 13-2: Parallel 8080 Timing Characteristics

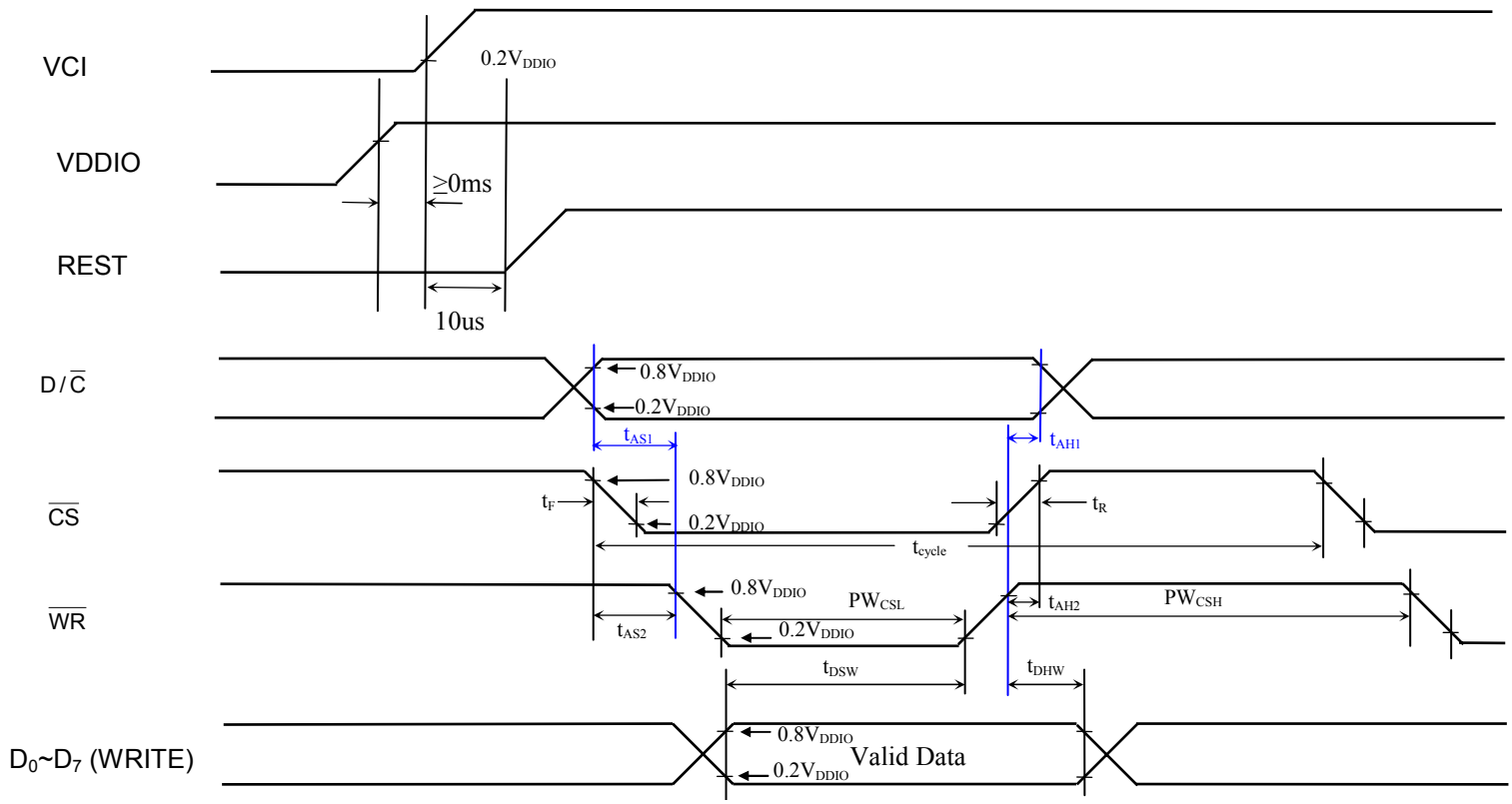
(T_A = -40 to 85°C, V_{DDIO} = 1.4V to 3.6V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time (write cycle)	75	-	-	ns
t_{cycle}	Clock Cycle Time (read cycle) (Based on VOL/VOH = 0.3*VDDIO/0.7*VDDIO)	450	-	-	ns
t_{AS1}	Address Setup Time between (R/$\overline{W}$) and D/$\overline{C}$	0	-	-	ns
t_{AH1}	Address Hold Time between (R/$\overline{W}$) and D/$\overline{C}$	0	-	-	ns
t_{AS2}	Address Setup Time between (R/$\overline{W}$) and $\overline{CS}$	0	-	-	ns
t_{AH2}	Address Hold Time between (R/$\overline{W}$) and $\overline{CS}$	0	-	-	ns
t_{DSW}	Data Setup Time (D0~D7, WRITE)	5	-	-	ns
t_{DHW}	Data Hold Time (D0~D7, WRITE))	5	-	-	ns
t_{ACC}	Data Access Time (D0~D7, READ)	250	-	-	ns
t_{OH}	Output Hold time (D0~D7, READ)	100	-	-	ns
PW_{CSL}	Pulse width /CS low (write cycle)	40	-	-	ns
PW_{CSH}	Pulse width /CS high (write cycle)	25	-	-	ns
PW_{CSL}	Pulse width /CS low (read cycle)	500	-	-	ns
PW_{CSH}	Pulse width /CS high (read cycle)	500	-	-	ns
t_R	Rise time	-	-	4	ns
t_F	Fall time	-	-	4	ns

Note: CS can be pulled low during the write cycle, only /RW is needed to be toggled

Figure 13-2: Parallel 8080-series Interface Timing Characteristics

Write Cycle



Remark: It's highly recommended that $\overline{RD}$ remains high for the whole write cycle

Read Cycle

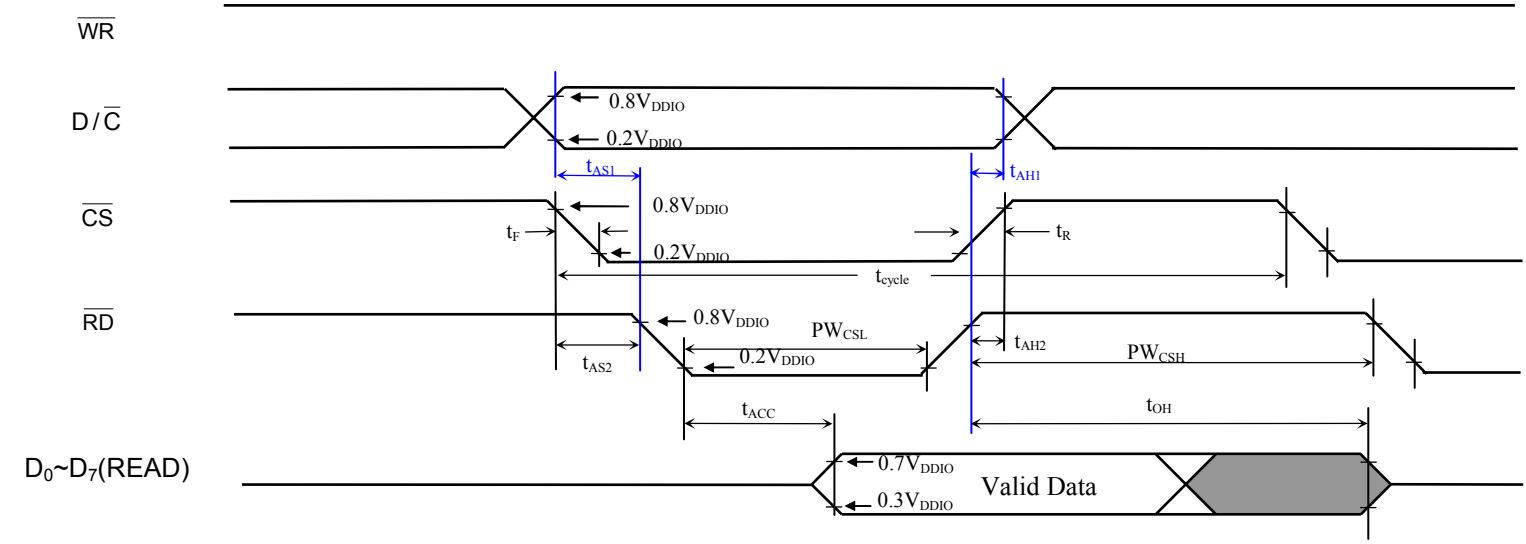


Table 13-3: Serial Timing Characteristics

(T_A = -40 to 85°C, V_{DDIO} = 1.4V to 3.6V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	77	-	-	ns
f_{CLK}	Serial Clock Cycle Time SPI Clock tolerance = +/- 2 ppm	-	-	15	MHz
t_{AS}	Register select Setup Time	4	-	-	ns
t_{AH}	Register select Hold Time	5	-	-	ns
t_{CSS}	Chip Select Setup Time	2	-	-	ns
t_{CSH}	Chip Select Hold Time	10	-	-	ns
t_{DSW}	Write Data Setup Time	5	-	-	ns
t_{OHW}	Write Data Hold Time	10	-	-	ns
t_{CLKL}	Clock Low Time	38	-	-	ns
t_{CLKH}	Clock High Time	38	-	-	ns
t_R	Rise time	-	-	4	ns
t_F	Fall time	-	-	4	ns

Figure 13-3: 4 wire Serial Timing Characteristics

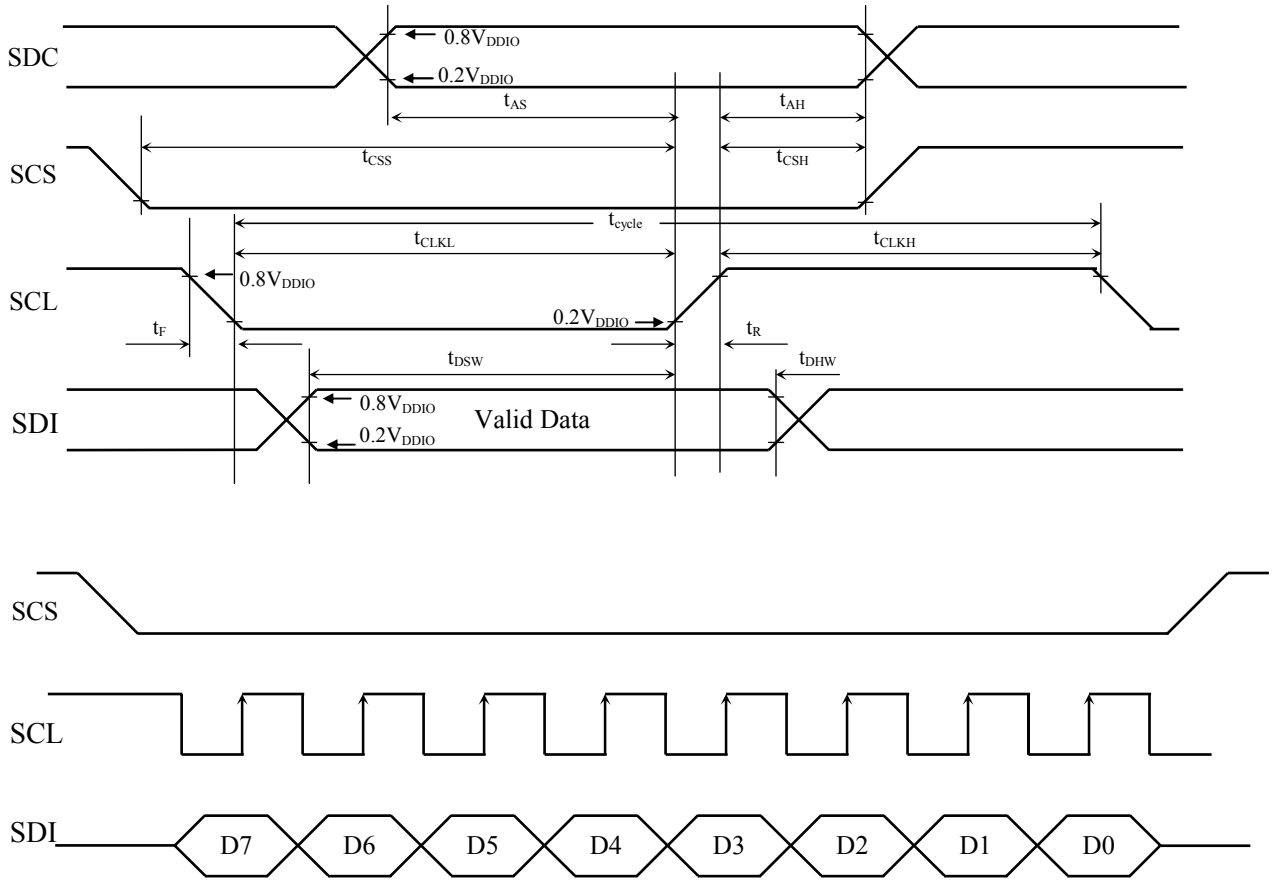


Table 13-4: RGB Timing Characteristics

(T_A = -40 to 85°C, V_{DDIO} = 1.4V to 3.6V)

Symbol	Parameter	Min	Typ	Max	Unit
f_{DOTCLK}	DOTCLK Frequency (70Hz frame rate)	1	5.5	8.2	MHz
t_{DOTCLK}	DOTCLK Period	122	182	1000	ns
t_{VSYS}	Vertical Sync Setup Time	20	-	-	ns
t_{VSYH}	Vertical Sync Hold Time	20	-	-	ns
t_{HSYS}	Horizontal Sync Setup Time	20	-	-	ns
t_{HSYH}	Horizontal Sync Hold Time	20	-	-	ns
t_{HV}	Phase difference of Sync Signal Falling Edge	0	-	320	t_{DOTCLK}
t_{CLK}	DOTCLK Low Period	61	-	-	ns
t_{CKH}	DOTCLK High Period	61	-	-	ns
t_{DS}	Data Setup Time	25	-	-	ns
t_{DH}	Data hold Time	25	-	-	ns

Note: External clock source must be provided to DOTCLK pin of SSD2119. The driver will not operate in absence of the clocking signal.

Figure 13-4: RGB Timing Characteristics

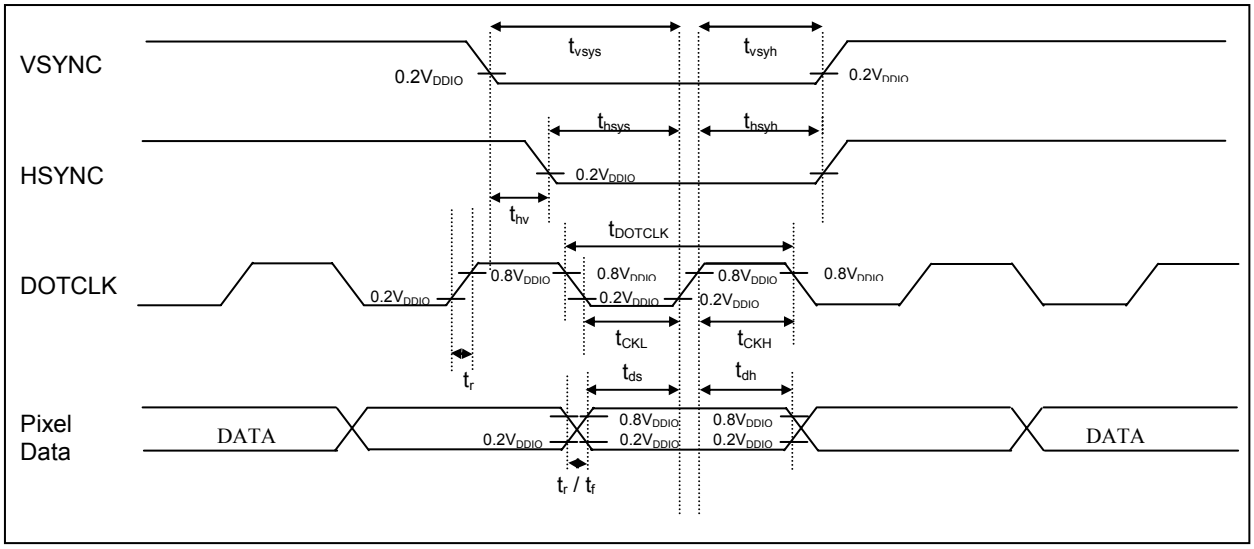


Figure 13-5: Power Up Sequence for RGB mode

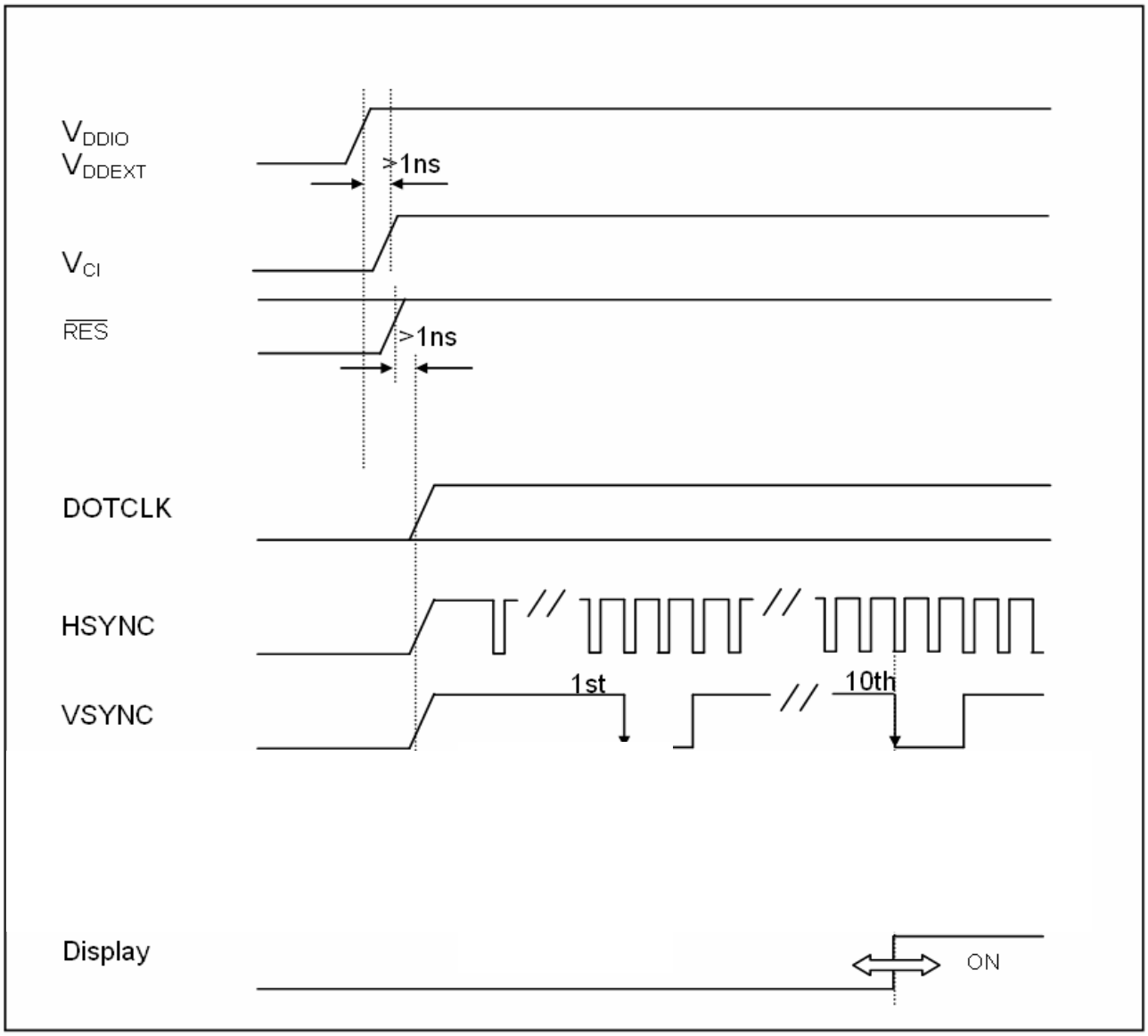
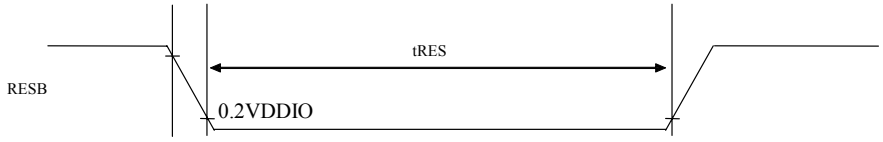


Table 13-5: Reset Timing

(T_A = -40 to 85°C, V_{DDIO} = 1.4V to 3.3V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{RES}	Reset pulse duration	15	-	-	us

Figure 13-6: Reset Timing Characteristics



14 GDDRAM Address

	RL=1	S0	S1	S2	S3	S4	S5	S6	S7	S8	…	S954	S955	S956	S957	S958	S959	
	RL=0	S959	S958	S957	S956	S955	S954	S953	S952	S951	…	S5	S4	S3	S2	S1	S0	
	BGR=0	R	G	B	R	G	B	R	G	B	…	R	G	B	R	G	B	Vertical address
	BGR=1	B	G	R	B	G	R	B	G	R	…	B	G	R	B	G	R	
TB=1	TB=0																	
G0	G239	0000H,0000H			0000H, 0001H			0000H, 0010H			…	0000H, 013EH			0000H, 013FH			0
G1	G238	0001H,0000H			0001H, 0001H			0001H, 0010H			…	0001H, 013EH			0001H, 013FH			1
G2	G237	0010H,0000H			0010H, 0001H			0010H, 0010H			…	0010H, 013EH			0010H, 013FH			2
G3	G236	0011H,0000H			0011H, 0001H			0011H, 0010H			…	0011H, 013EH			0011H, 013FH			3
G4	G235	0100H,0000H			0100H, 0001H			0100H, 0010H			…	0100H, 013EH			0100H, 013FH			4
.	.	.			.			.			.	.			.			.
.	.	.			.			.			.	.			.			.
.	.	.			.			.			.	.			.			.
G236	G3	013CH, 0000H			013CH, 0001H			013CH, 0010H			…	00ECH, 013EH			00ECH, 013FH			236
G237	G2	013DH, 0000H			013DH, 0001H			013DH, 0010H			…	00EDH, 013EH			00EDH, 013FH			237
G238	G1	013EH, 0000H			013EH, 0001H			013EH, 0010H			…	00EEH, 013EH			00EEH, 013FH			238
G239	G0	013FH, 0000H			013FH, 0001H			013FH, 0010H			…	00EFH, 013EH			00EFH, 013FH			239

Horizontal address	0	1	2	…	318	319

Remark : The address is in 00xxH,0yyyH format, where yyy is the vertical address and xx is the horizontal address

15 INTERFACE MAPPING

15.1 Interface Setting

Table 15-1: Interface setting and data bus setting

PS3	PS2	PS1	PS0	Interface Mode	Data bus input	Data bus output
0	0	0	0	16-bit 6800 parallel interface	D[17:10], D[8:1]	D[17:10], D[8:1]
0	0	0	1	8-bit 6800 parallel interface	D[17:10]	D[17:10]
0	0	1	0	16-bit 8080 parallel interface	D[17:10], D[8:1]	D[17:10], D[8:1]
0	0	1	1	8-bit 8080 parallel interface	D[17:10]	D[17:10]
1	0	1	0	18-bit 8080 parallel interface	D[17:0]	D[17:0]
1	0	1	1	9-bit 8080 parallel interface	D[17:9]	D[17:9]
1	0	0	0	18-bit 6800 parallel interface	D[17:0]	D[17:0]
1	0	0	1	9-bit 6800 parallel interface	D[17:9]	D[17:9]

15.1.1 6800-series System Bus Interface

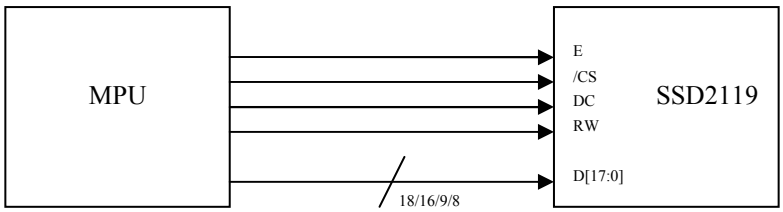


Table 15-2: The Function of 6800-series parallel interface

PS3	PS2	PS1	PS0	Interface Mode	Data bus	RW	E	DC	/CS	Operation
0	0	0	0	16-bit 6800 parallel interface	D[17:10], D[8:1]	1	↴	0	0	Read 8-bit command
						1	↴	1	0	Read 16-bit parameters or status*
						0	↴	0	0	Write 8-bit command
						0	↴	1	0	Write 16-bit display data
0	0	0	1	8-bit 6800 parallel interface	D[17:10]	1	↴	0	0	Read 8-bit command
						1	↴	1	0	Read 8-bit parameters or status*
						0	↴	0	0	Write 8-bit command
						0	↴	1	0	Write 8-bit display data
1	0	0	0	18-bits 6800 parallel interface	D[17:0]	1	↴	0	0	Read 8-bit command
						1	↴	1	0	Read 18-bit parameters or status*
						0	↴	0	0	Write 8-bit command
						0	↴	1	0	Write 18-bit display data
1	0	0	1	9-bits 6800 parallel interface	D[17:9]	1	↴	0	0	Read 8-bit command
						1	↴	1	0	Read 9-bit parameters or status*
						0	↴	0	0	Write 8-bit command
						0	↴	1	0	Write 9-bit display data

* A dummy read is required before the first actual display data read

15.1.2 8080-series System Bus Interface

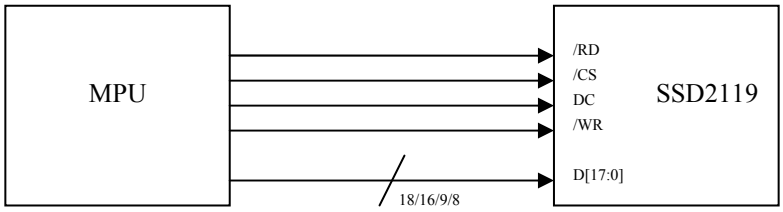


Table 15-3: The Function of 8080-series parallel interface

PS3	PS2	PS1	PS0	Interface Mode	Data bus	/WR	/RD	DC	/CS	Operation
0	0	1	0	16-bit 8080 parallel interface	D[17:10], D[8:1]	1	0	0	0	Read 8-bit command
						1	0	1	0	Read 8-bit parameters or status*
						0	1	0	0	Write 8-bit command
						0	1	1	0	Write 16-bit display data
0	0	1	1	8-bit 8080 parallel interface	D[17:10]	1	0	0	0	Read 8-bit command
						1	0	1	0	Read 8-bit parameters or status*
						0	1	0	0	Write 8-bit command
						0	1	1	0	Write 8-bit display data
1	0	1	0	18-bit 8080 parallel interface	D[17:0]	0	1	0	0	Read 8-bit command
						1	0	1	0	Read 8-bit parameters or status*
						0	1	0	0	Write 8-bit command
						0	1	1	0	Write 18-bit display data
1	0	1	1	9-bit 8080 parallel interface	D[17:9]	1	0	0	0	Read 8-bit command
						1	0	1	0	Read 8-bit parameters or status*
						0	1	0	0	Write 8-bit command
						0	1	1	0	Write 9-bit display data

* A dummy read is required before the first actual display data read

15.2 Mapping for Writing an Instruction

		Hardware pins																	
Interface	**Cycle**	**D17**	**D16**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
18 bits		IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	x	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0	x
16 bits		IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8		IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0	
9 bits	1st	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	x									
	2nd	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0	x									
8 bits	1st	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8										
	2nd	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0										

Remark : x Don't care bits
Not connected pins

15.3 Mapping for Writing Pixel Data

			Hardware pins																
Interface	**Color mode**	**Cycle**	**D17**	**D16**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
18 bits	**262k**		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
16 bits	**262k**	1st	R5	R4	R3	R2	R1	R0	x	x		G5	G4	G3	G2	G1	G0	x	x	
		2nd	B5	B4	B3	B2	B1	B0	x	x		R5	R4	R3	R2	R1	R0	x	x	
		3rd	G5	G4	G3	G2	G1	G0	x	x		B5	B4	B3	B2	B1	B0	x	x	
		1st	R5	R4	R3	R2	R1	R0	x	x		G5	G4	G3	G2	G1	G0	x	x	
		2nd	x	x	x	x	x	x	x	x		B5	B4	B3	B2	B1	B0	x	x	
		1st	R5	R4	R3	R2	R1	R0	x	x		G5	G4	G3	G2	G1	G0	x	x	
		2nd	B5	B4	B3	B2	B1	B0	x	x		x	x	x	x	x	x	x	x	
	65k		R4	R3	R2	R1	R0	G5	G4	G3		G2	G1	G0	B4	B3	B2	B1	B0	
9 bits	**262k**	1st	R5	R4	R3	R2	R1	R0	G5	G4	G3									
		2nd	G2	G1	G0	B5	B4	B3	B2	B1	B0									
8 bits	**262k**	1st	R5	R4	R3	R2	R1	R0	x	x										
		2nd	G5	G4	G3	G2	G1	G0	x	x										
		3rd	B5	B4	B3	B2	B1	B0	x	x										
	65k	1st	R4	R3	R2	R1	R0	G5	G4	G3										
		2nd	G2	G1	G0	B4	B3	B2	B1	B0										

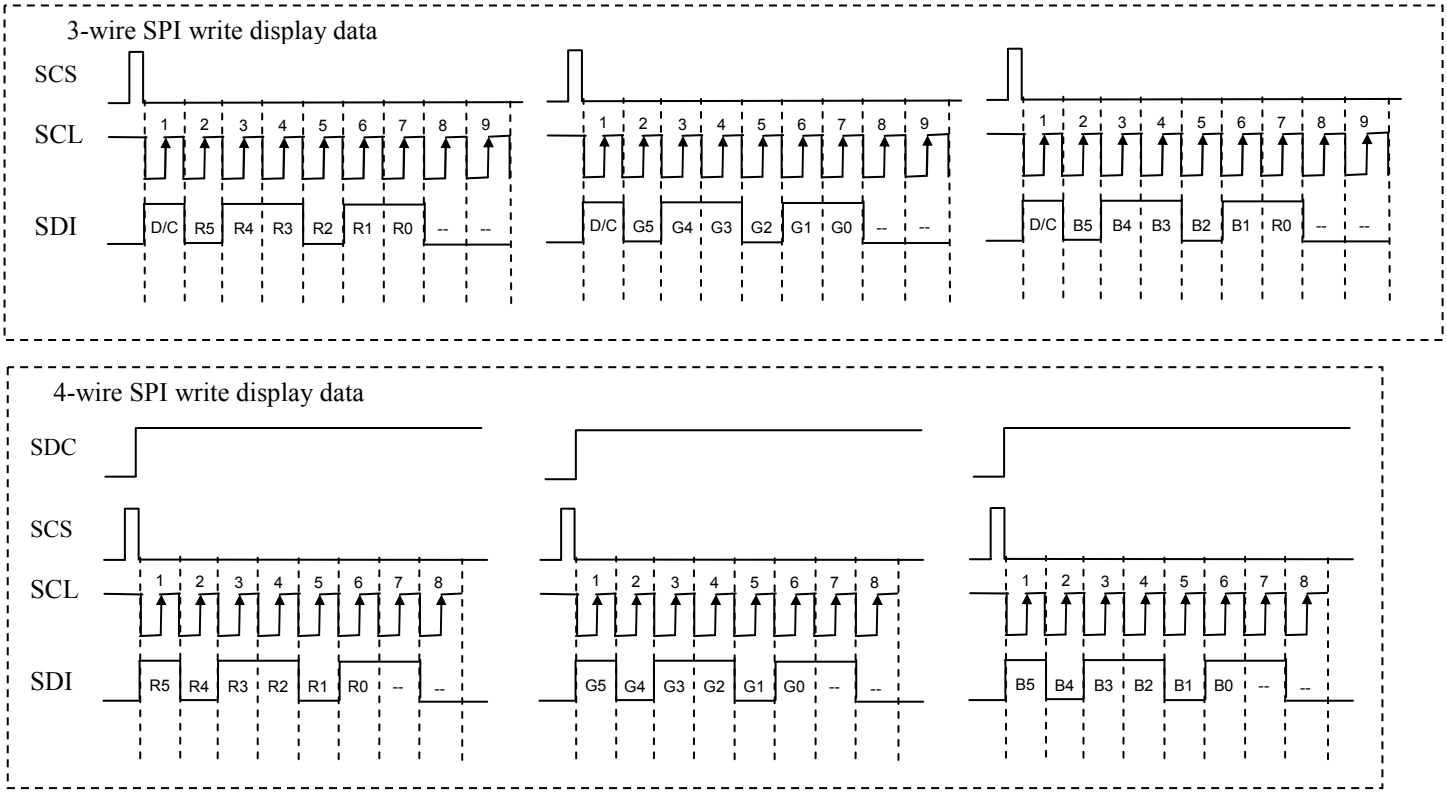
Remark : x Don't care bits
Not connected pins

15.4 Mapping for Writing Pixel Data in generic mode

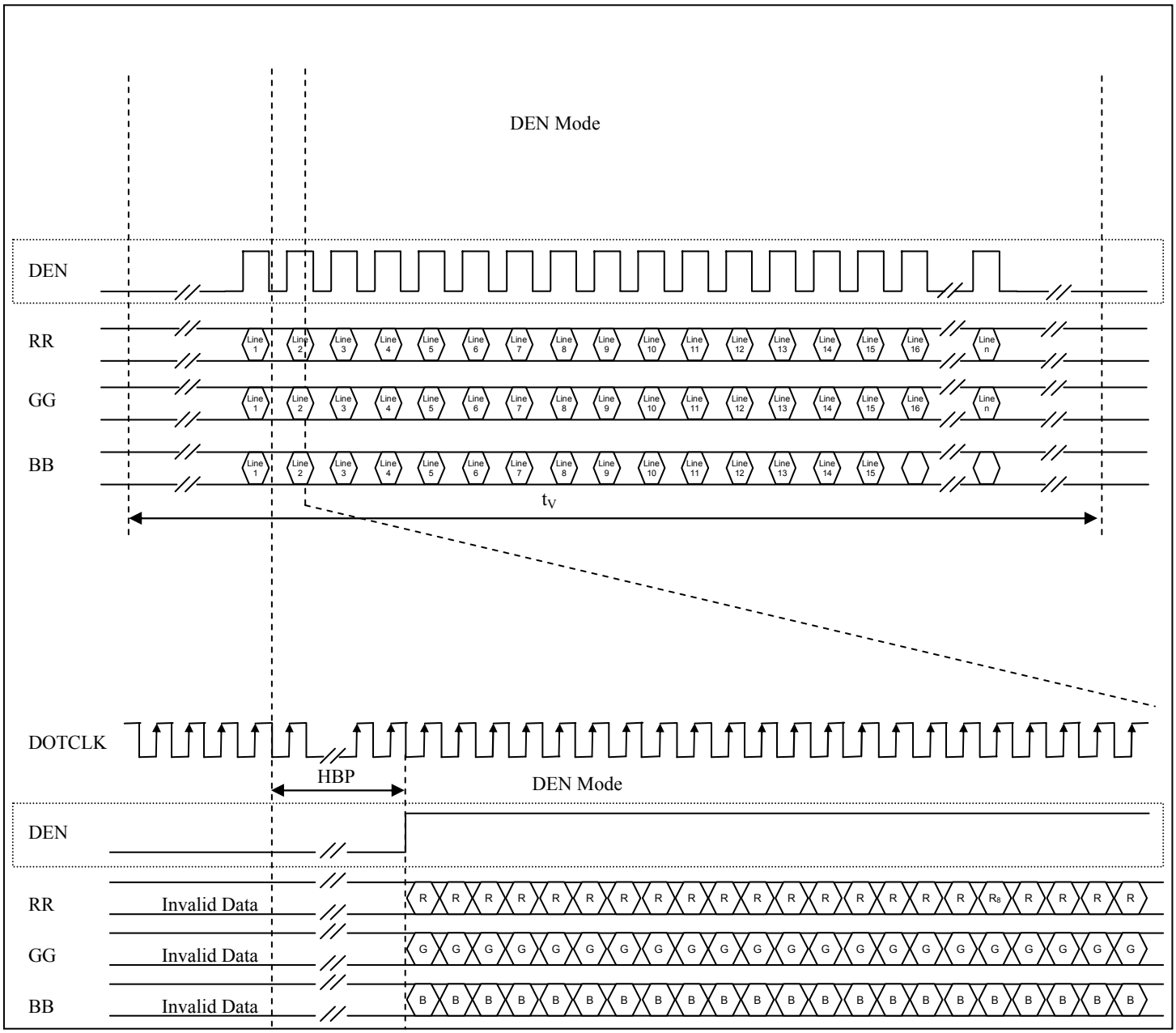
Interface	**Color mode**	**Cycle**	**D17**	**D16**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
18-bit RGB PS=[0110]	**262k**	-	RR5	RR4	RR3	RR2	RR1	RR0	GG5	GG4	GG3	GG2	GG1	GG0	BB5	BB4	BB3	BB2	BB1	BB0
18-bit RGB PS=[0110]	**65k**	-	RR4	RR3	RR2	RR1	RR0	RR4	GG5	GG4	GG3	GG2	GG1	GG0	BB4	BB3	BB2	BB1	BB0	BB4
16-bit RGB PS=[0101]	**65k**	-	RR4	RR3	RR2	RR1	RR0	GG5	GG4	GG3		GG2	GG1	GG0	BB4	BB3	BB2	BB1	BB0	
9-bit RGB	**262k**	1st	RR5	RR4	RR3	RR2	RR1	RR0	GG5	GG4	GG3									
		2nd	BB5	BB4	BB3	BB2	BB1	BB0	GG2	GG1	GG0									
6-bit RGB	**262k**	1st	RR5	RR4	RR3	RR2	RR1	RR0												
		2nd	GG5	GG4	GG3	GG2	GG1	GG0												
		3rd	BB5	BB4	BB3	BB2	BB1	BB0												

Remark: Not Connected pins

15.5 Mapping for Writing Pixel Data in SPI mode

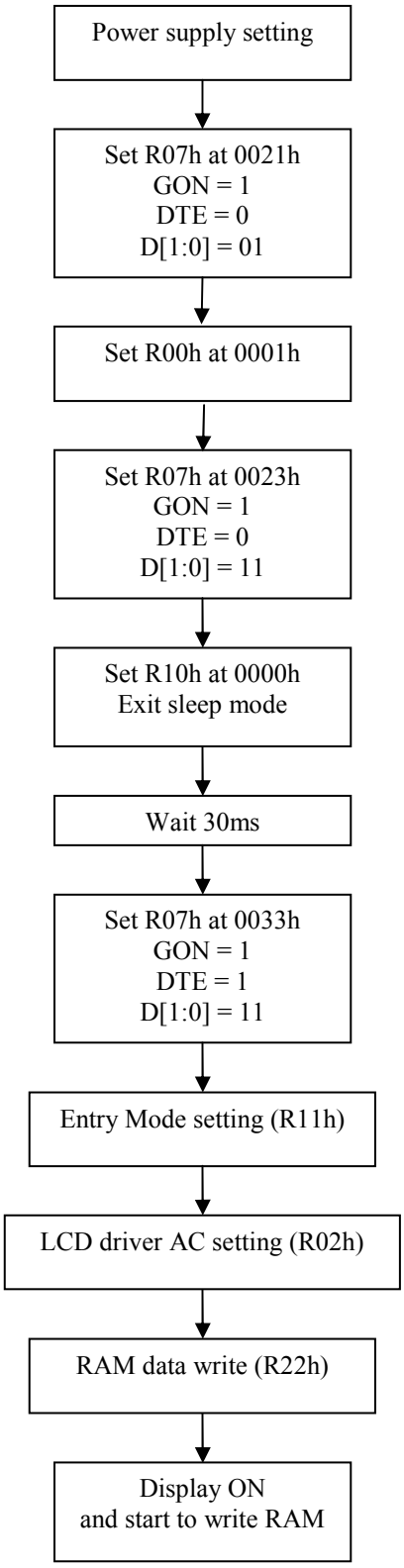


15.6 Mapping for Writing Pixel Data in RGB DEN mode

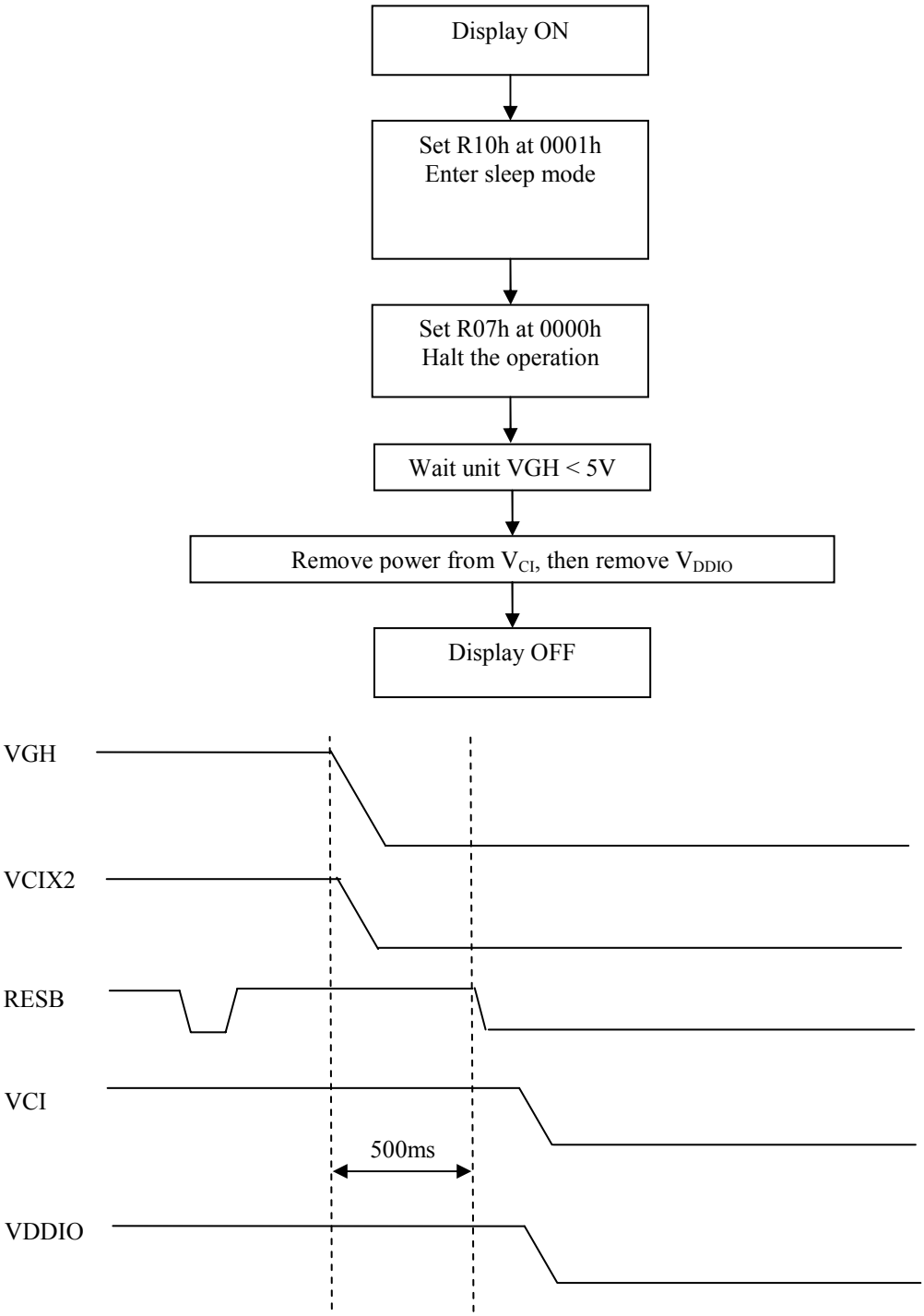


16 DISPLAY SETTING SEQUENCE

16.1 Display ON Sequence

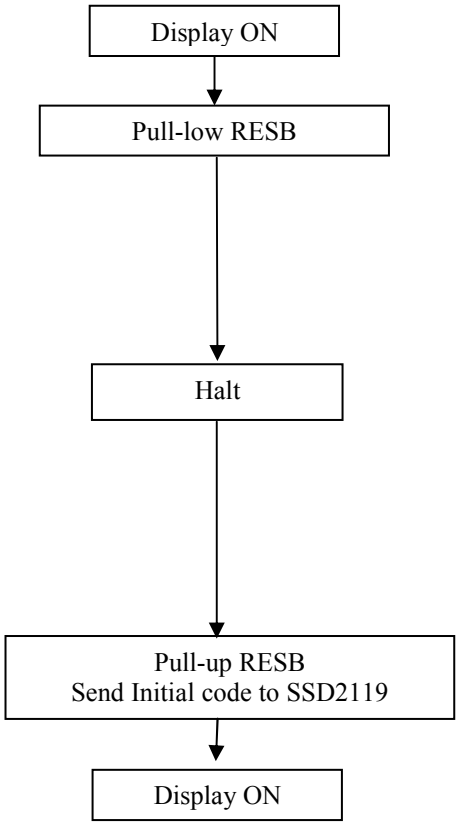


16.2 Display OFF Sequence

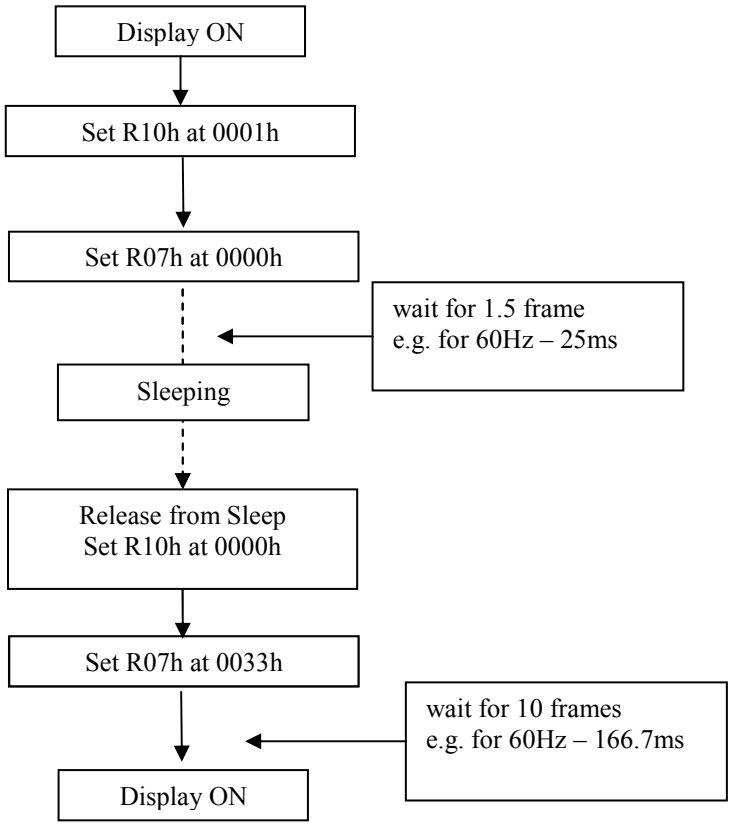


Note:
1. VDDIO should be the last to fall, or VCI/VDDIO could be power off at the same time
2. If OTP is active in the application, the OTP programming voltage should be turned off and cap discharged before VCI/VDDIO are turned off.

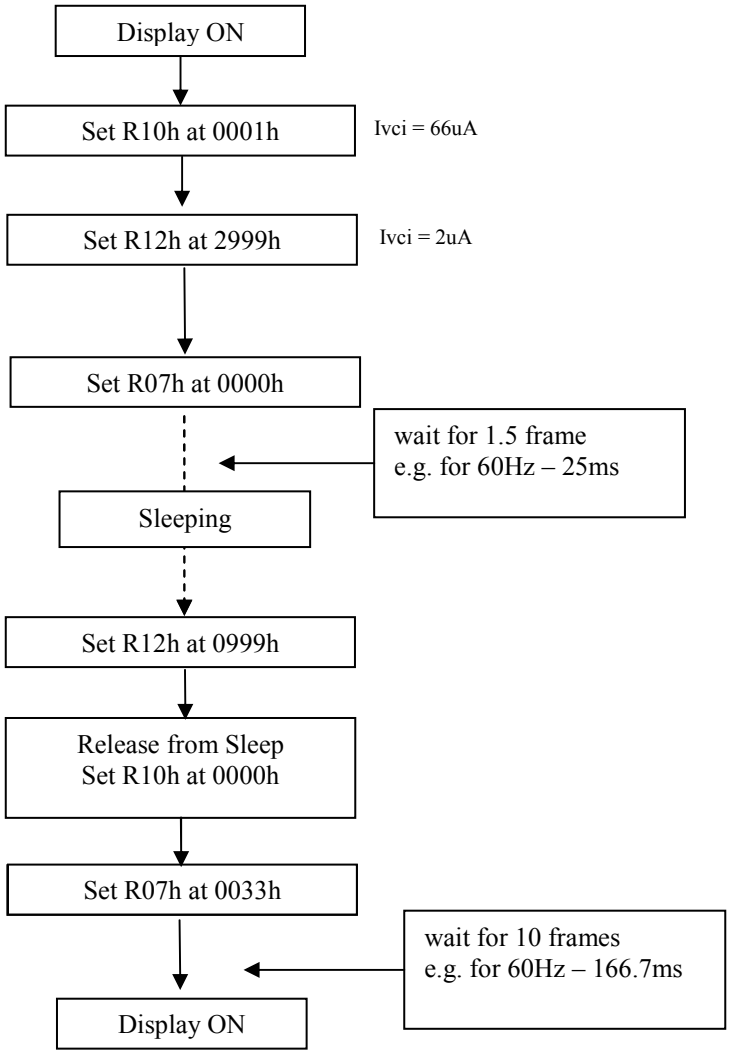
16.3 Halt Sequence



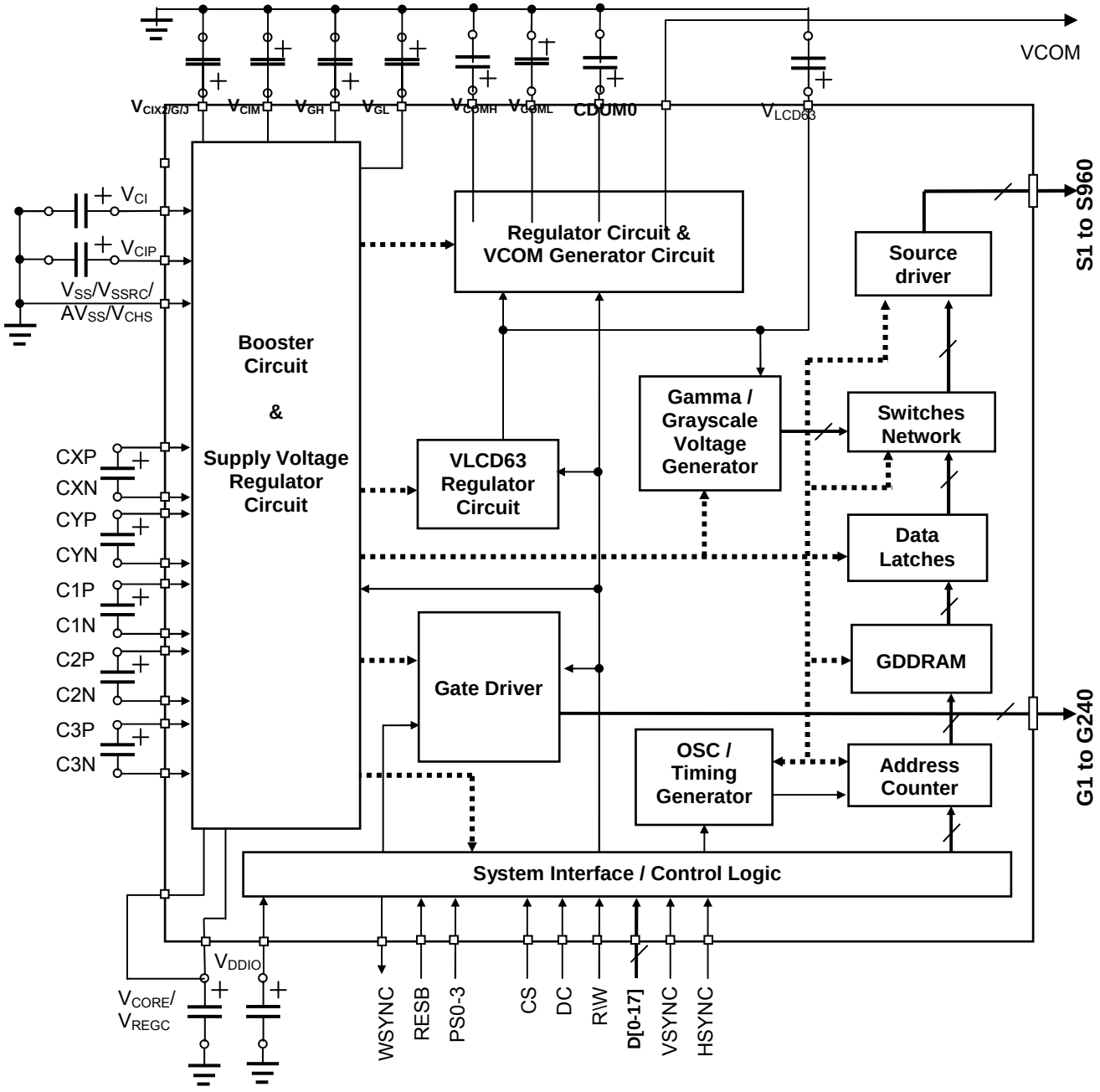
16.4 Sleep Mode Display Sequence



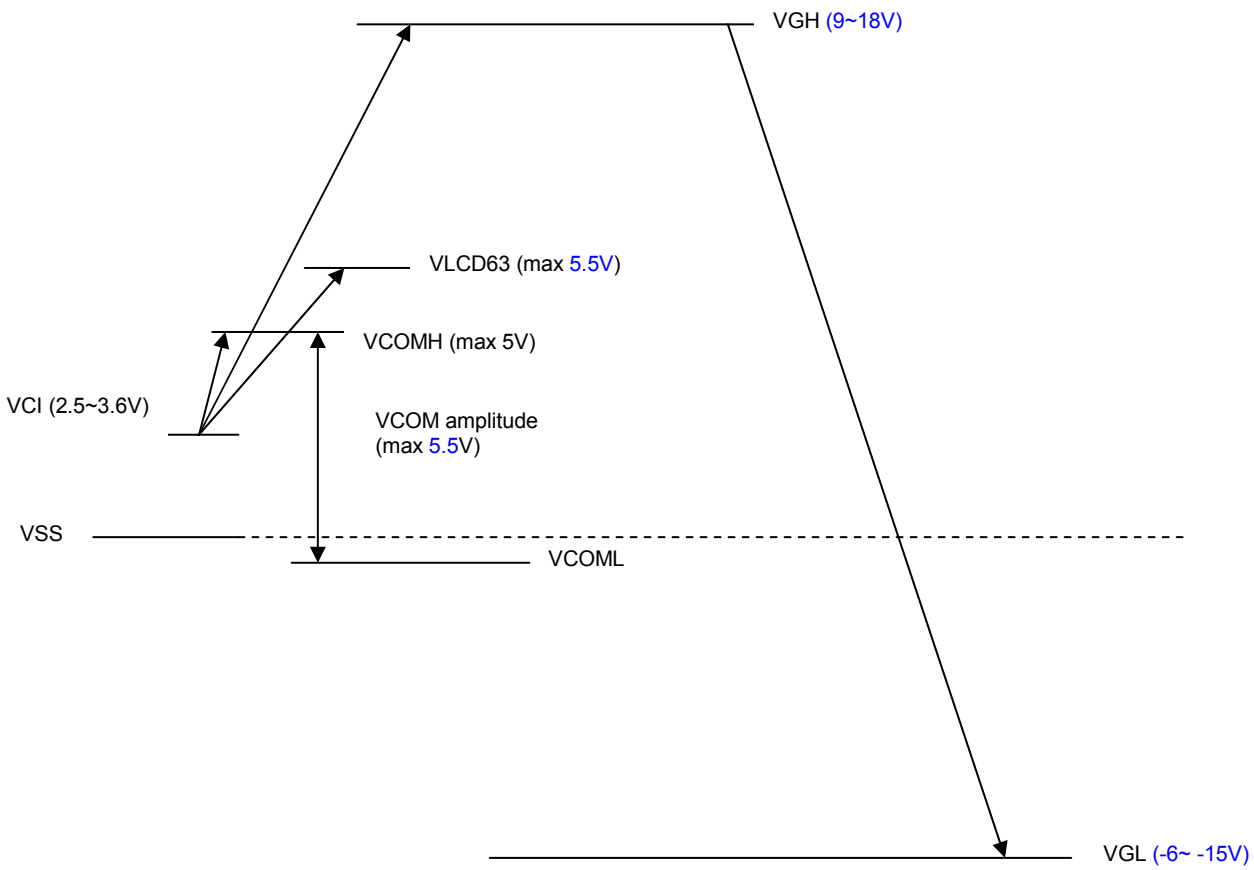
16.5 Deep Sleep Mode Display Sequence



17 POWER SUPPLY BLOCK DIAGRAM



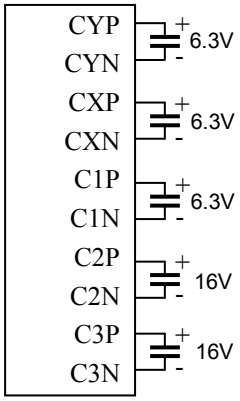
18 SSD2119 OUTPUT VOLTAGE RELATIONSHIP



Note: VGH-VGL<30V_{p-p}

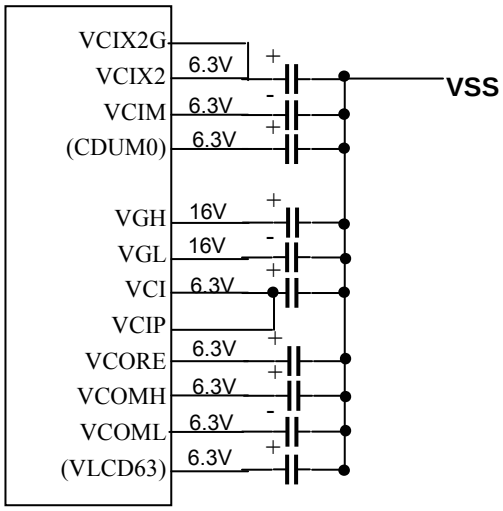
19 APPLICATION CIRCUIT

Figure 19-1: Booster Capacitors



All capacitors
0.1 ~ 0.22uF (0.22uF for better stability)

Figure 19-2: Filtering and Charge Sharing Capacitors



Mandatory requirement on external components for SSD2119 is 10 capacitors.
VCIX2, VCIM, VGH, VGL, VCI, VCORE, VCOMH, VCOML
C1P/C1N, C2P/C2N, C3P/C3N, CYP/CYN, CXP/CXN

Remark:
Capacitor for VCIX2 = 2.2uF
VCI should be separated with VCIP at ITO layout to provide noise free path.
VSS should be separated with VCHS, AVSS and VSSRC at ITO layout to provide noise free path.
All other capacitors 1.0uF ~ 2.2uF (2.2uF is preferred for better display quality and power consumption.)

(Optional capacitors)
VLCD63, capacitors are for stability
Capacitors on CDUM0 are for power saving.

Figure 19-3: Panel Connection Example

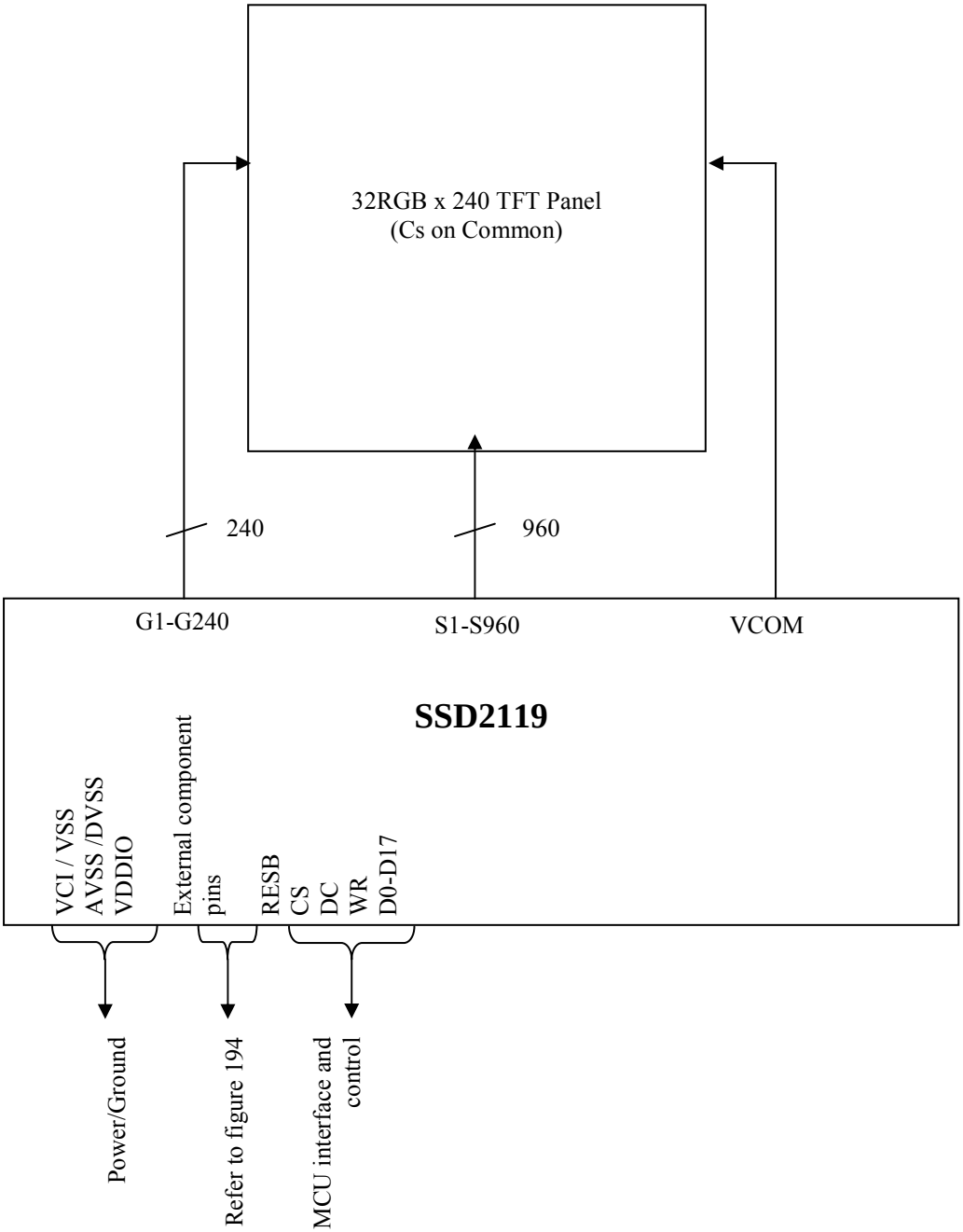
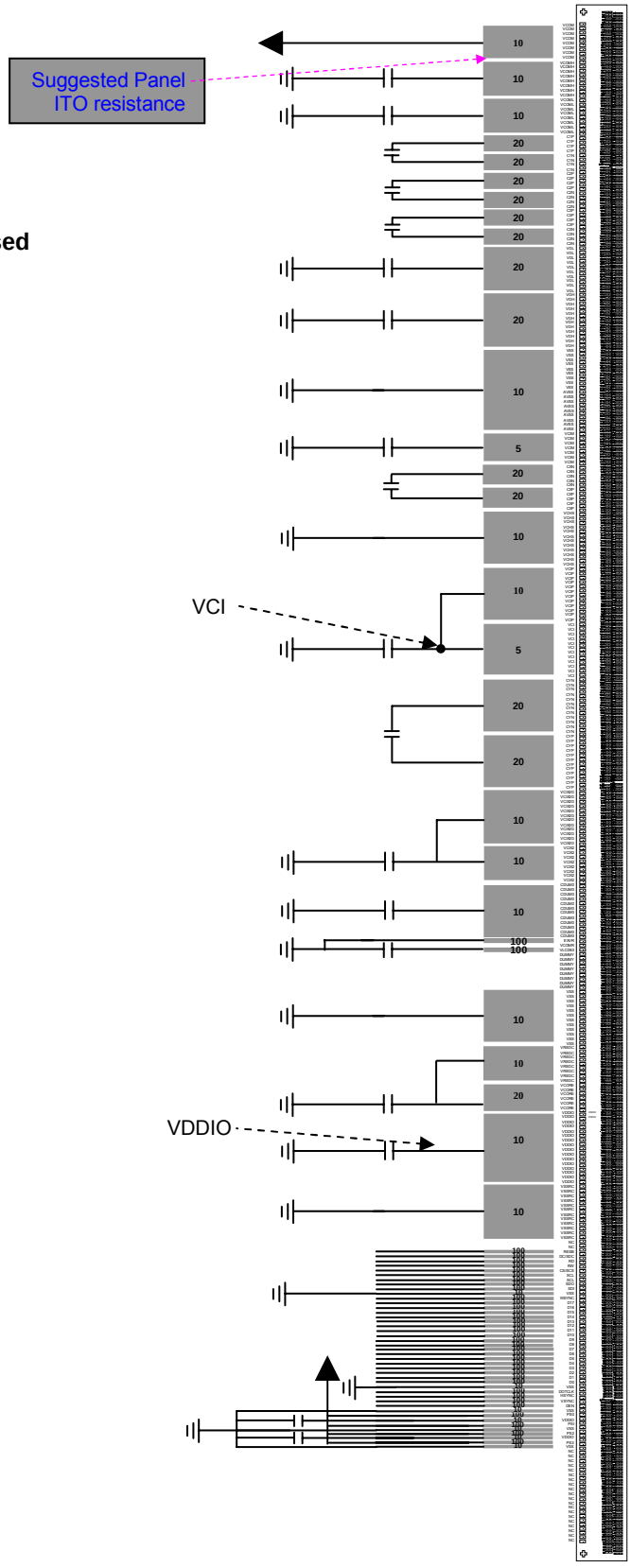


Figure 19-4: ITO and FPC connection example



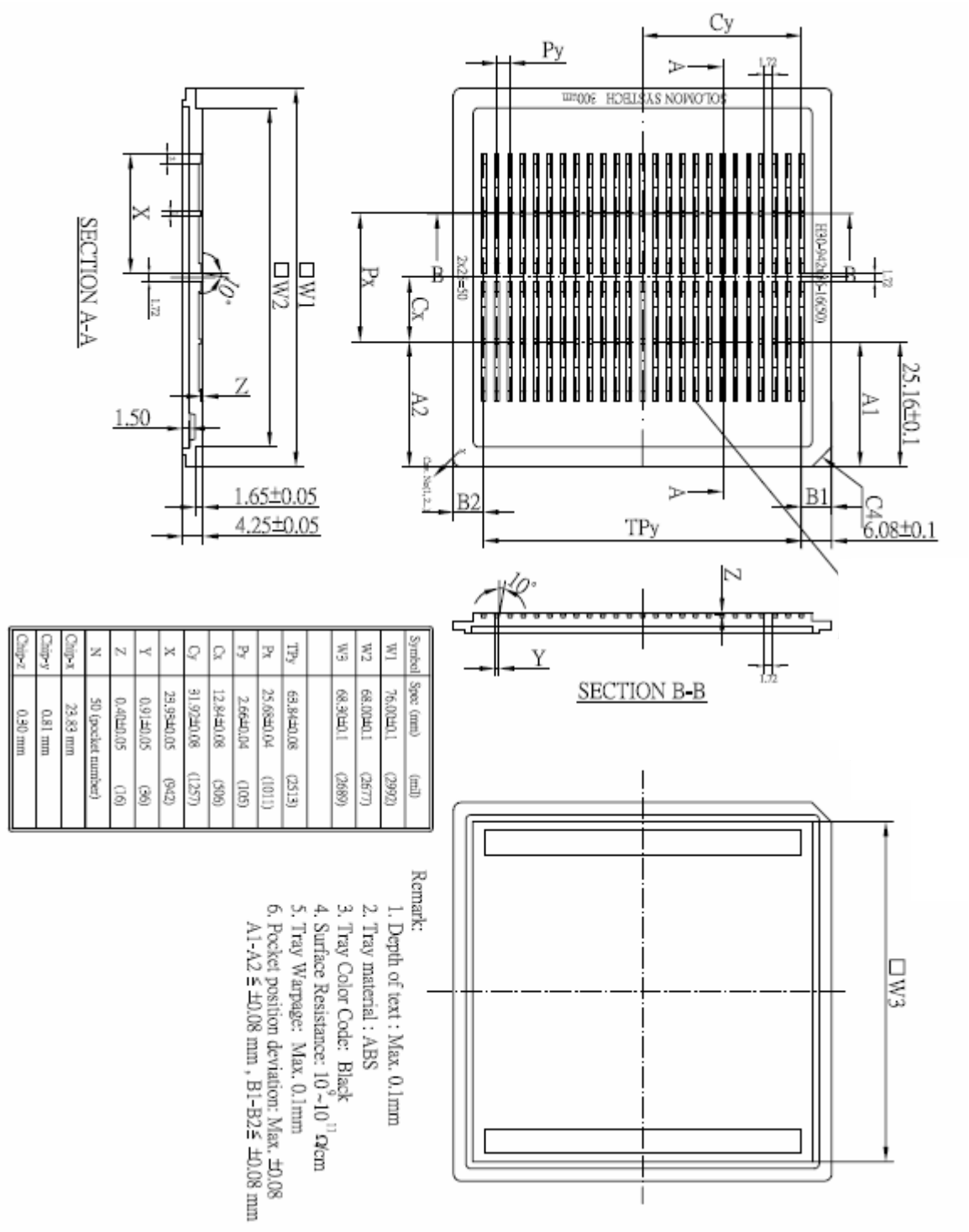
Operating conditions:

- **Cs on common structure is used**
- **Color filter mapping**
- **Normal white panel is used**

20 PACKAGE INFORMATION

20.1 Chip Tray Information

SSD2119Z7



Symbol	Spec (mm)	(mil)
W1	76.00±0.1	(2992)
W2	68.00±0.1	(2677)
W3	68.30±0.1	(2689)
TPy	63.84±0.08	(2513)
Px	25.68±0.04	(1011)
Py	2.66±0.04	(105)
Cx	12.84±0.08	(506)
Cy	31.92±0.08	(1257)
X	23.95±0.05	(942)
Y	0.91±0.05	(36)
Z	0.40±0.05	(16)
N	50 (pocket number)	
Chip-x	23.83 mm	
Chip-y	0.81 mm	
Chip-z	0.30 mm	

Remark:

1. Depth of text : Max. 0.1mm
2. Tray material : ABS
3. Tray Color Code: Black
4. Surface Resistance: 10^{9}~10^{11} Ω/cm
5. Tray Warpage: Max. 0.1mm
6. Pocket position deviation: Max. ±0.08
   A1-A2 ≤ ±0.08 mm , B1-B2≤ ±0.08 mm

21 OTP DETAIL

Fresh die

1) **Example 1 - VCMR[5:0] is as default**

A fresh SSD2119 will have the OTP register default value of OTPR[5:0]=0x00 and default value of VCMR[5:0]=0x2B, which corresponds to base values [110110] from the 6 least significant bits.

VCMR[5:0]	1	0	1	0	1	1
OTPR[5:0]	0	0	0	0	0	0
VCOMH = VCMR XOR OTPR	1	0	1	0	1	1

2) **Example 2 - VCM[5:0] is adjusted and nOTP=1**

nOTP=1 will override the default VCOMH value and is used together with VCM[5:0] to find out the optimal value against flickering.

Purpose VCMR[5:0] and OTPR[5:0] is the same as example 2.

For example, when nOTP=1 and VCM[5:0]=0x2B which corresponding to [110110], the resultant VCOMH will equal VCM regardless the value of VCMR XOR OTPR.

VCM[5:0]	1	0	1	0	1	1
VCOMH = VCM	1	0	1	0	1	1

The new VCOMH value will become, 0x2B

(Please be noted that preceding 10'b is added to the result so as to have uniformity as R1E command is sent.)

Program OTP

When nOTP=1, R1E command is mainly used to find out the optimal value against flickering. The OTPR will be programmed as below.
(The equivalent VCOMH value is simply VCM[5:0] if nOTP is 1)

Example - VCMR[5:0] is as default, target VCOMH value is equivalent to VCM[5:0] = 0x30.

When R1E-0x00B0 is sent, VCM[5:0] will be [110000]. The OTPR will be the XOR result of VCM[5:0] and VCMR[5:0]. In this case, VCMR[5:0] is the default = 0x2B.

VCM[5:0]	1	1	0	0	0	0
VCMR[5:0]	1	0	1	0	1	1
OTPR[5:0]	0	1	1	**0**	**1**	1

The result in OTPR means bit 4, bit3, bit 1 and bit 0 in OTPR[5:0] are programmed.

Solomon Systech reserves the right to make changes without notice to any products herein. Solomon Systech makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Solomon Systech assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any, and all, liability, including without limitation consequential or incidental damages. “Typical” parameters can and do vary in different applications. All operating parameters, including “Typical” must be validated for each customer application by the customer’s technical experts. Solomon Systech does not convey any license under its patent rights nor the rights of others. Solomon Systech products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Solomon Systech product could create a situation where personal injury or death may occur. Should Buyer purchase or use Solomon Systech products for any such unintended or unauthorized application, Buyer shall indemnify and hold Solomon Systech and its offices, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Solomon Systech was negligent regarding the design or manufacture of the part.

All Solomon Systech Products complied with six (6) hazardous substances limitation requirement per European Union (EU) “Restriction of Hazardous Substance (RoHS) Directive (2002/95/EC)” and China standard “电子信息产品污染控制标识要求 (SJ/T11364-2006)” with control Marking Symbol  . Hazardous Substances test report is available upon requested.

http://www.solomon-systech.com